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E3ABP30534M 000
E3AZP30554 000

Technical Training

JSS DATA PROCESSOR AND DISPLAY MAINTENANCE

HMP-1116 FUNCTIONAL BLOCK DIAGRAMS

MAY 1986

USAF TECHNICAL TRAINING SCHOOL
3300th Technical Training WING
Keesler Air Force Base, Mississippi

Designed For ATC Course Use

DO NOT USE ON THE JOB

PHILOSOPHY

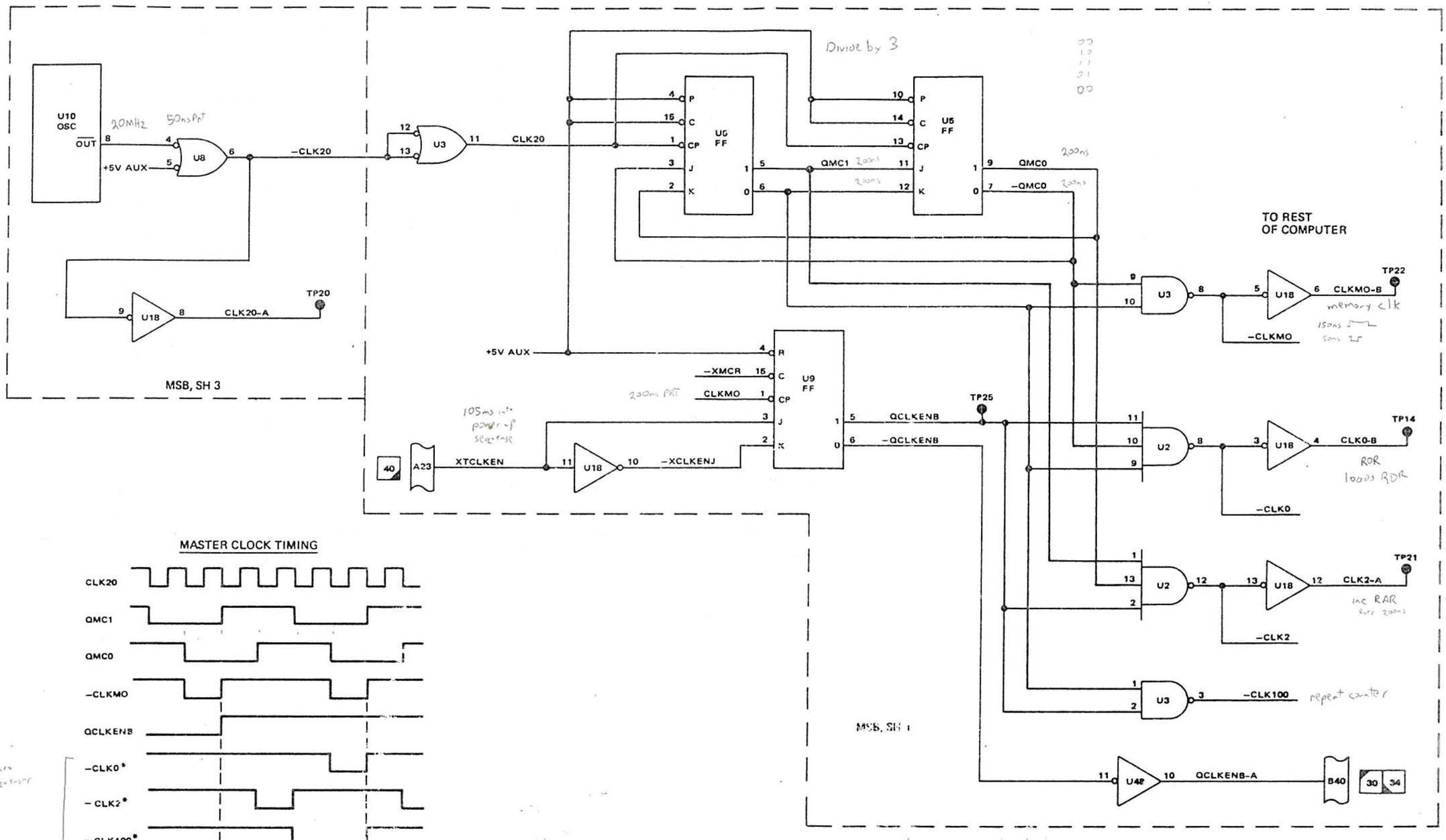
The philosophy of the wing emerges from a deep concern for individual Air Force men and women and the need to provide highly trained and motivated personnel to sustain the mission of the Air Force. We believe the abilities, worth, self-respect, and dignity of each student must be fully recognized. We believe each must be provided the opportunity to pursue and master an occupational specialty to the full extent of individual's capabilities and aspirations, for the immediate and continuing benefit of the individual, the Air Force, and the country. To these ends, we provide opportunities for individual development of initial technical proficiency, on-the-job training in challenging job assignments, and follow-on growth as supervisors. In support of this individual development, and to facilitate maximum growth of its students, the wing encourages and supports the professional development of its faculty and administrators, and actively promotes innovation through research and the sharing of concepts and material with other educational institutions.

6.0 FUNCTIONAL SCHEMATICS

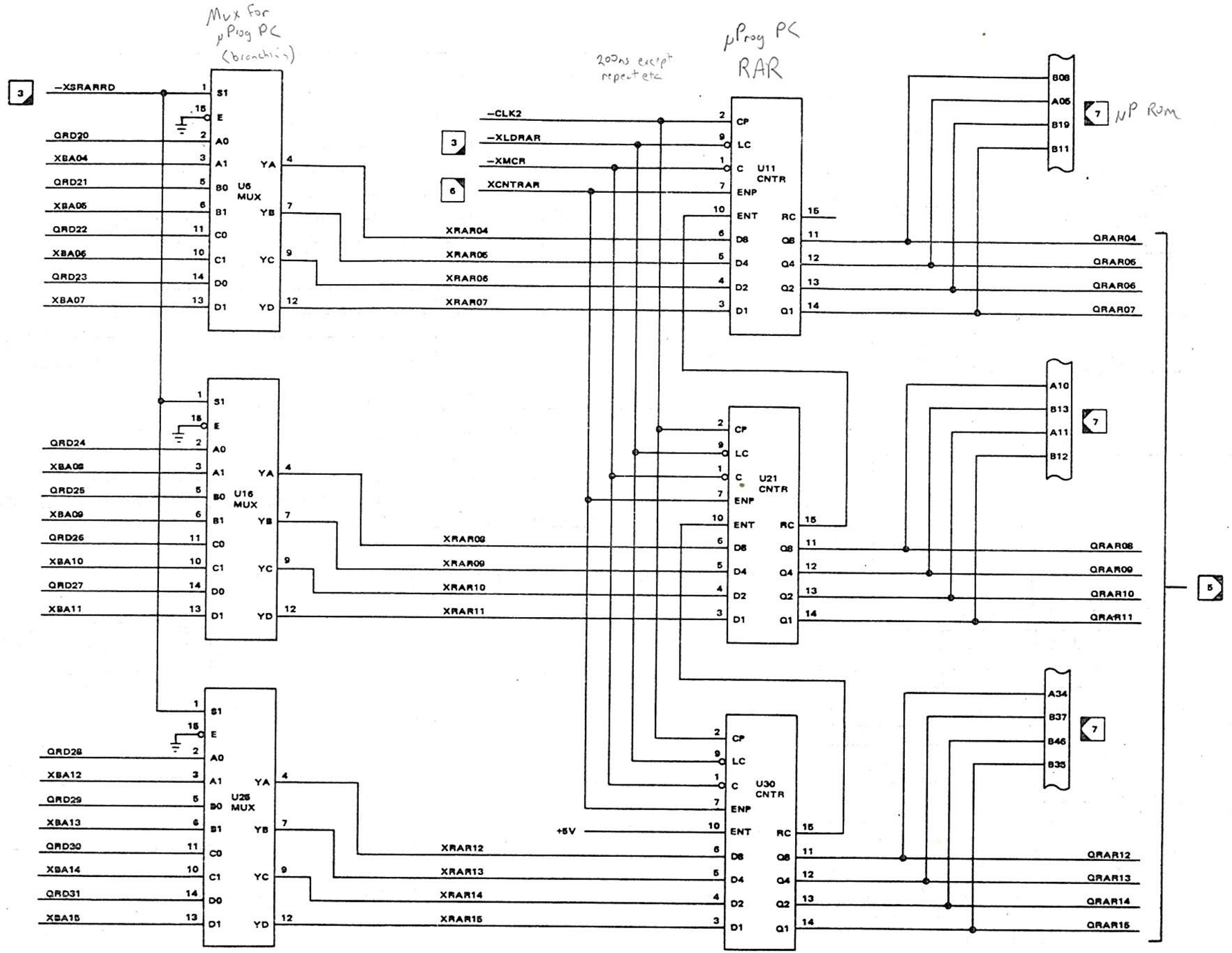
The following 44 pages contain the Functional Schematics for the HMP-1116. The Functional Schematics can be related to both the overall block diagrams in Chapters 3, 10 and 11, and the schematics in Volume 2 of the Tech. Manual.

The blocks in the block diagrams in Chapters 3 (Processor), 10 (Memory) and 11 (Power) contain reference numbers. The reference number(s) in a block refer to the page(s) in the Functional Schematics which show the details of that block.

The Functional Schematics have references to the schematics in Volume 2 of the Tech. Manual. For example, the reference MSB, SH. 1 tells you that the function is located on sheet 1 of the schematics of the MSB card.

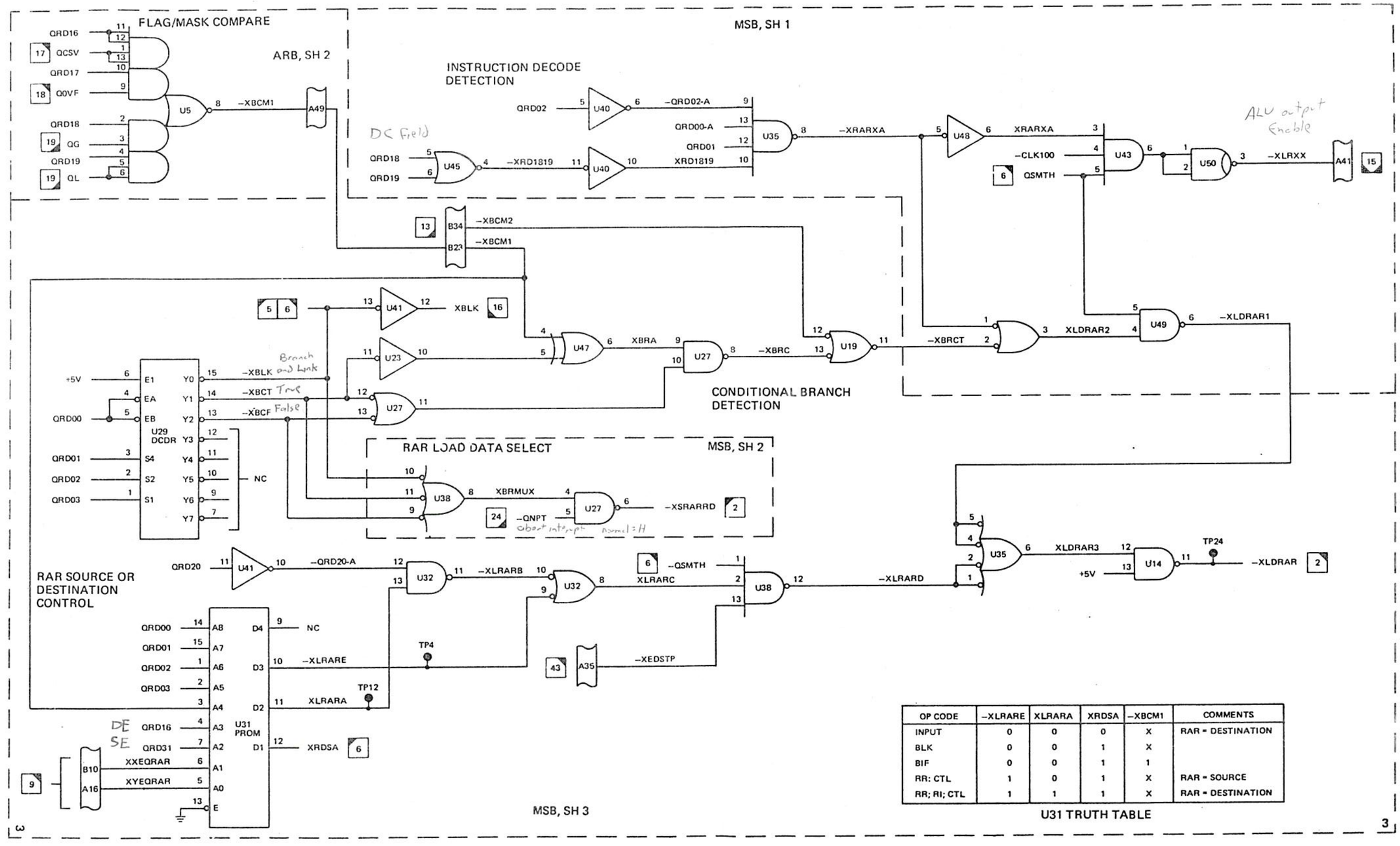

U10
OSC
OUT
20MHz
50ns Prt
+5V AUX
U8
-CLK20
U3
CLK20
MSB, SH 3
U18
CLK20-A
TP20
Divide by 3
U6
FF
U5
FF
QMC1
QMC0
-QMC0
200ns
TO REST
OF COMPUTER
TP22
CLKMO-B
memory clk
150ns
50ns
-CLKMO
+5V AUX
U9
FF
-XMCR
CLKMO
200ns PRT
105ms init
power up
sequence
TP25
QCLKENB
-QCLKENB
40
A23
XTCLKEN
U18
-XCLKENJ
U2
TP14
CLK0-B
ROR
loads RDR
-CLK0
TP21
CLK2-A
inc RAR
-CLK2
U3
-CLK100
repeat counter
MSB, SH 1
U42
QCLKENB-A
B40
30
34
Keyswitch 'On' sends signals only to
memory with a 105ms delay
1
CLOCK GENERATOR
MASTER CLOCK TIMING
CLK20
QMC1
QMC0
-CLKMO
QCLKENB
micro
sequencer
-CLK0*
-CLK2*
-CLK100*
ONE CLOCK CYCLE
* INHIBITED WHEN QCLKENB LO
*=inhibited when
QCLKENB is low

MSB, SH 2



2

ROM ADDRESS REGISTER



OP CODE	–XLRARE	XLRARA	XRDSA	–XBCM1	COMMENTS
INPUT	0	0	0	X	RAR = DESTINATION
BLK	0	0	1	X	
BIF	0	0	1	1	
RR: CTL	1	0	1	X	RAR = SOURCE
RR; RI; CTL	1	1	1	X	RAR = DESTINATION

U31 TRUTH TABLE

RAR BRANCH AND LOAD CONTROL

IFCH Fetch
SFDC execute

IFCH Fetch
PFDC second Fetch
SFDC execute

Only During CONTROL micro Instruc!

(See KDA-5042 pg 5-9,10)
Software Execution Cycle

Proms Provide Start Address's
For Micro Program

ERC, SH 1

(KDA-5042 pg 4-19)

Pri Q19	Q19	DC	does
X	0	00	NOP
1	0	01	PFDC
X	1	0	10	SFDC
X	1	1	11	IFCH (interrupt check)

Normally low

6 A36 -QSMTH 5 U14 6 QSMTH-A

(KDA-5042 pg 4-10)

QRD00 1
QRD01 2
-QRD02 13
U13 12
13 25 Control XCTL
2 U15 12
1 -CLK100 13
-XDREN

Instruction Size
0 = halfword (16)
1 = Fullword (32)

+5V 6 EI
4 EA
5 EB
U35 DCDR
Y0 15 NC
Y1 14 -XESFB
Y2 13 -XESFA
Y3 12 -XESFC
Y4 11 NC
Y5 10
Y6 9
Y7 7

11 B42 QIR01 3
GRD18 2
GRD19 1
24 B31 -QNPT-A

-XEIFA 5
-XEIFB 3
U34
4
6 -XEIFCH

Secondary Function Decode
U34 8 -XESFDC TP26
TP29 -XEPFDC
TP28 -XEIFCH

B39 B31 -XESFDC Execute
B40 B29 -XEPFDC Data Fetch
A10 A06 -XEIFCH Instruction Fetch

Software Abort
(KDA-5042 pg 3-5)

ERM, SH 3

11 -QIR12 2
-QIR13 1
-QIR14 4
-QIR15 5
U25 6 -XNDXZRO A46

(KDA-5042 pg 5-11)
Micro Code pg 19,20

02C Inst. Fetch
02E Brkpoint Add
033 Norm Interrupts
02F Abort
(KDA 5042 pg 5-10/11)

Priority
1st Interrupts
2nd Breakpoints
3rd IFetch

24 -XINTRPT 13 U29 12 XINTRPT
R4 1k +5V

U6 PROM
U10 PROM
A8 A7 A6 A5 A4 A3 A2 A1 A0
D4 D3 D2 D1
E

27 B08 -SBKPTEN
24 A08 -QNPT-A
Abort
(KDA-5042 pg 3-5)

ERM, SH 1

9 10 U23 8 -XEIFPF

1 G1 U30 BFR 3 5 7 9
2 D1 Y1
4 D2 Y2
6 D3 Y3
10 D4 Y4
Puts Φs in MSB in IFetch or PFDC

ERM, SH 4

Only in SFDC

11 QIR00
QIR01
QIR02
QIR03
QIR04
QIR05
QIR06
12 QIR07
QPSW 31

U50 PROM
A8 A7 A6 A5 A4 A3 A2 A1 A0
D4 D3 D2 D1
E

XBA04
XBA05
XBA06
XBA07

goes to A-bus as a 12 bit Micro Code Start Address

Only in SFDC

U45 PROM
XBA08
XBA09
XBA10
XBA11

Only in SFDC

U46 PROM
XBA12
XBA13
XBA14
XBA15

Only in PFDC

U41 PROM

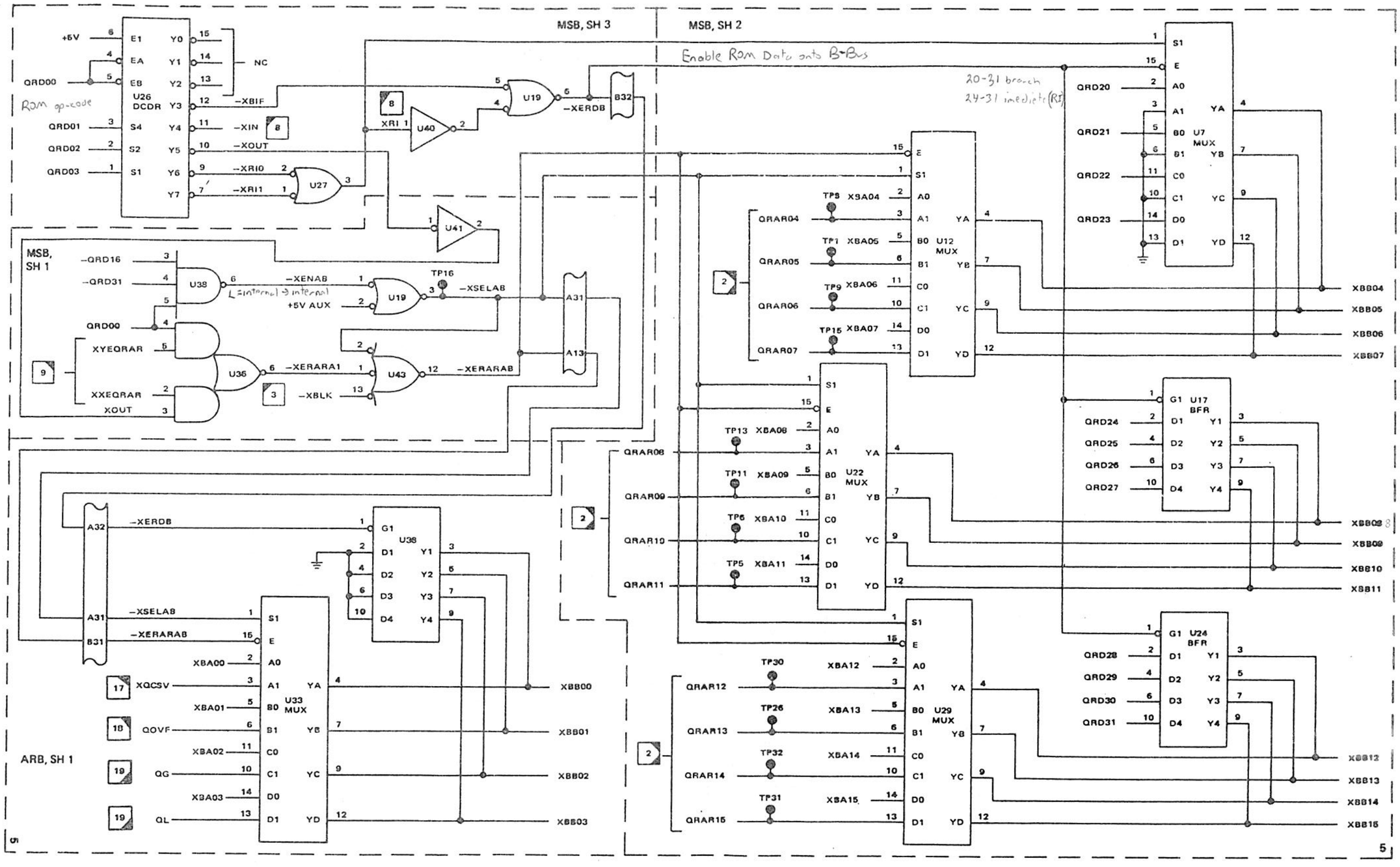
Puts Φs in PFDC

1 G1 U26 BFR 3 5 7 9
2 D1 Y1
4 D2 Y2
6 D3 Y3
10 D4 Y4

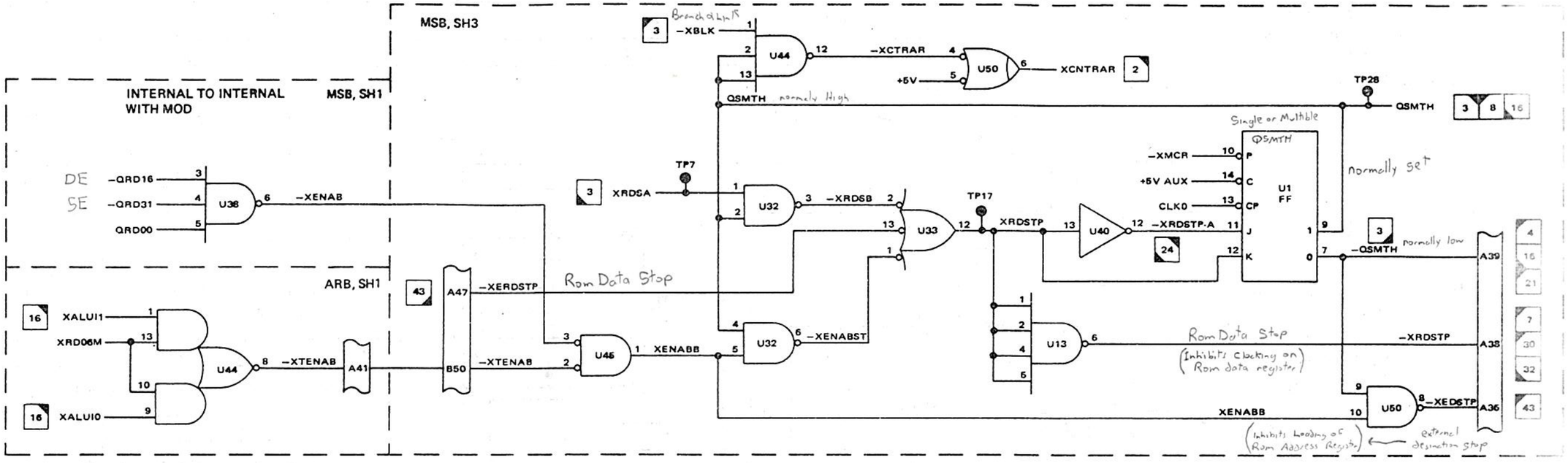
820 -XNDXZRO

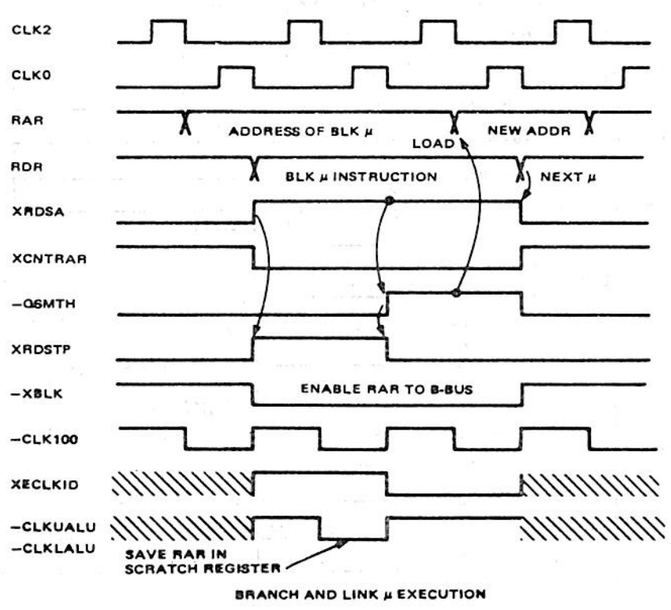
INSTRUCTION DECODE ROM

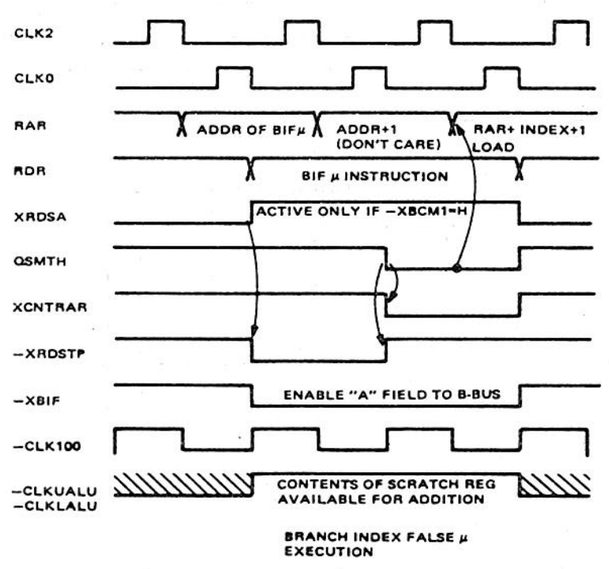
Used if KUK or KAK is specified as source and when moving data Internal reg → Internal reg thru byte manipulator

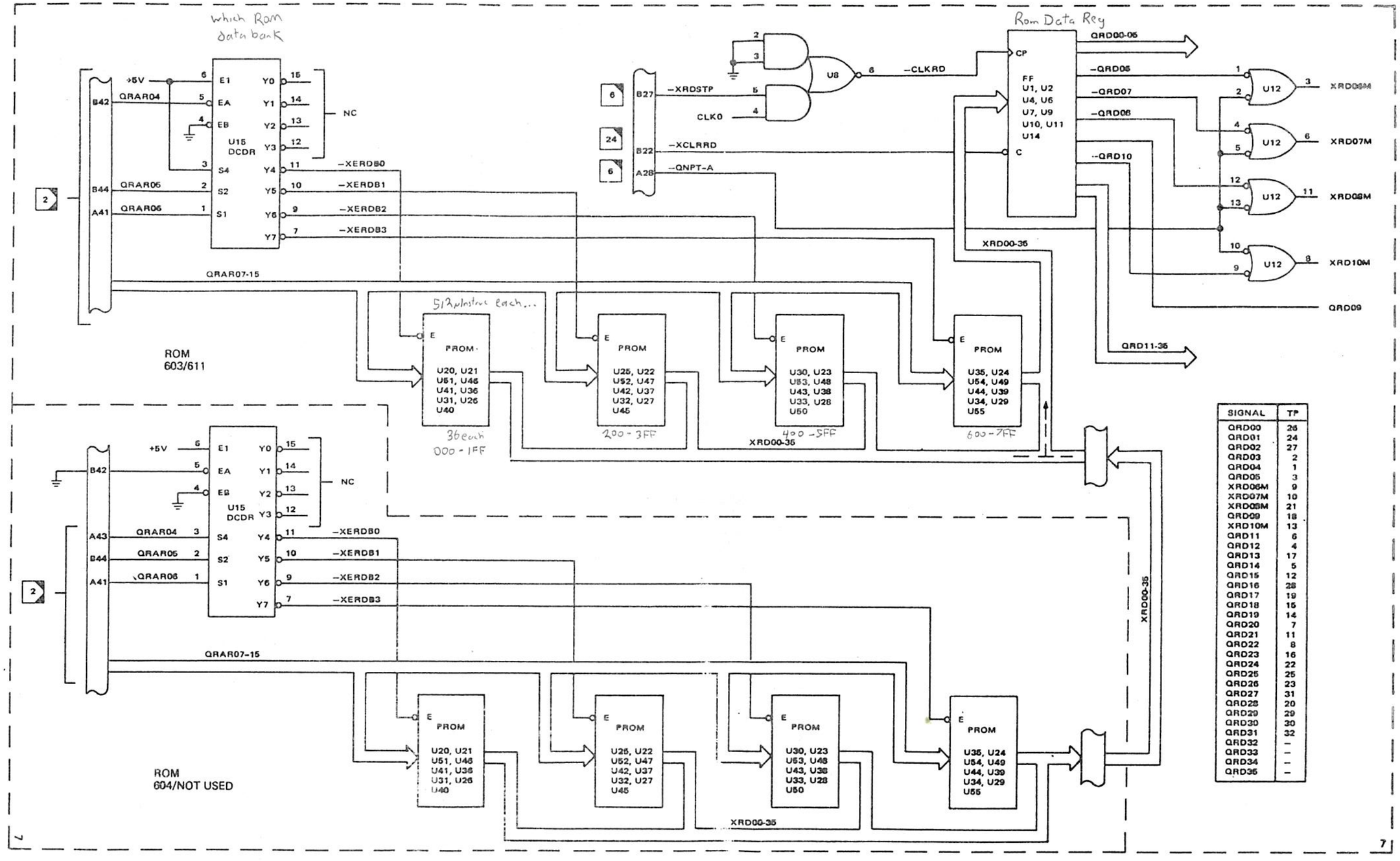


ROM ADDRESS B-BUS MUX

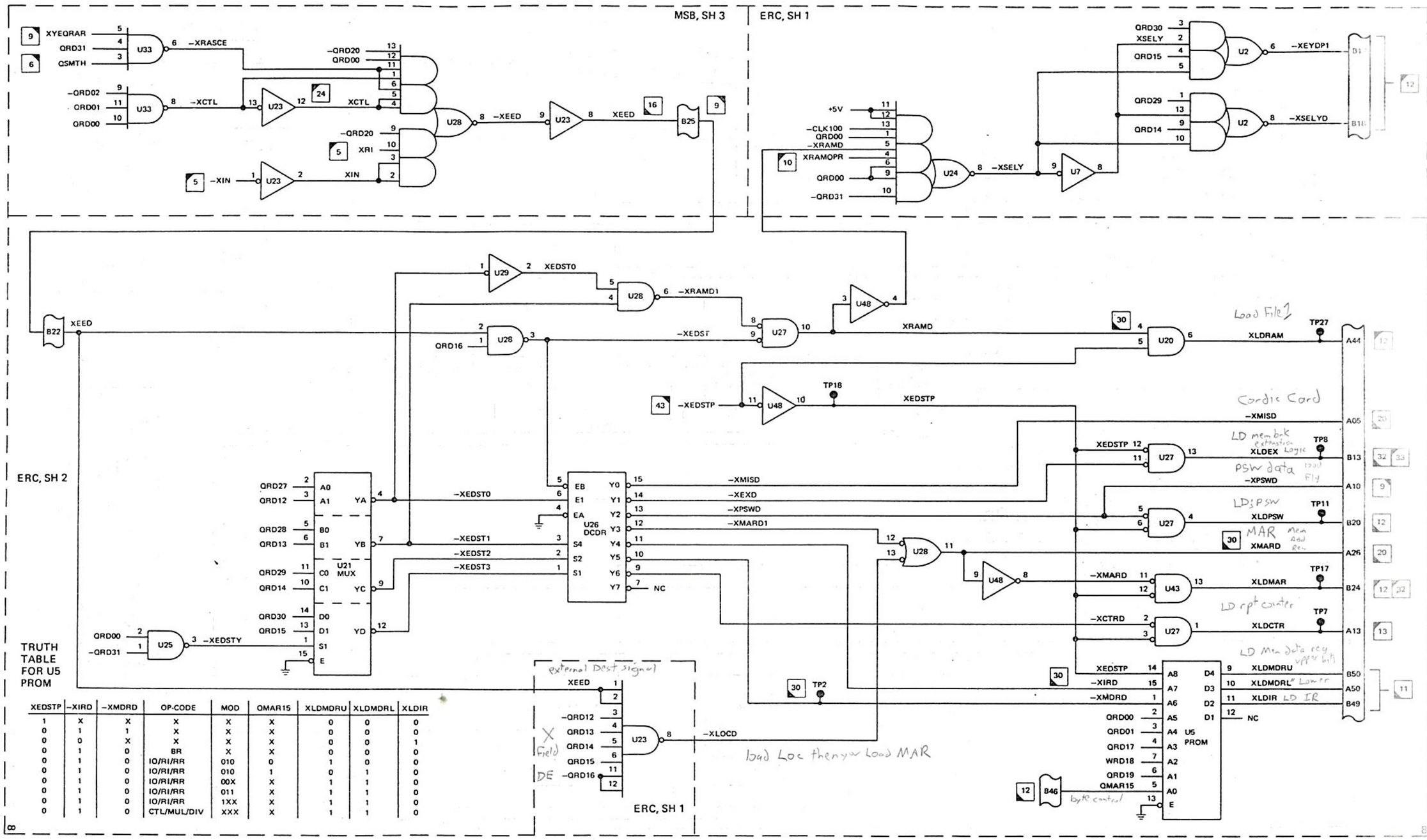

MSB, SH3
INTERNAL TO INTERNAL
WITH MOD
MSB, SH1
ARB, SH1
DE
SE
-QRD16
-QRD31
QRD00
U38
-XENAB
XALUI1
XRD06M
XALUI0
U44
-XTENAB
A41
A47
-XERDSTP
B50
-XTENAB
Rom Data Stop
U45
XENABB
-XBLK
U44
-XCTRAR
+5V
U50
XCNTRAR
QSMTH normally High
TP28
QSMTH
Single or Multible
XRDSA
TP7
U32
-XRDSB
U33
TP17
XRDSTP
U40
-XRDSTP-A
U1
FF
-XMCR
+5V AUX
CLK0
P
C
CP
J
K
normally set
-QSMTH
normally low
U32
-XENABST
U13
Rom Data Stop
(Inhibits clocking on
Rom data register)
-XRDSTP
XENABB
U50
-XED6TP
(Inhibits Loading of
Rom Address Register)
external destination Stop
A39
A38
A36


CLK2
CLK0
RAR
RDR
XRDSA
XCNTRAR
-QSMTH
XRDSTP
-XBLK
-CLK100
XECLKID
-CLKUALU
-CLKLALU
ADDRESS OF BLK μ
NEW ADDR
LOAD
BLK μ INSTRUCTION
NEXT μ
ENABLE RAR TO B-BUS
SAVE RAR IN
SCRATCH REGISTER
BRANCH AND LINK μ EXECUTION


CLK2
CLK0
RAR
RDR
XRDSA
QSMTH
XCNTRAR
-XRDSTP
-XBIF
-CLK100
-CLKUALU
-CLKLALU
ADDR OF BIFμ
ADDR+1
(DON'T CARE)
RAR+ INDEX+1
LOAD
BIF μ INSTRUCTION
ACTIVE ONLY IF -XBCM1=H
ENABLE "A" FIELD TO B-BUS
CONTENTS OF SCRATCH REG
AVAILABLE FOR ADDITION
BRANCH INDEX FALSE μ
EXECUTION

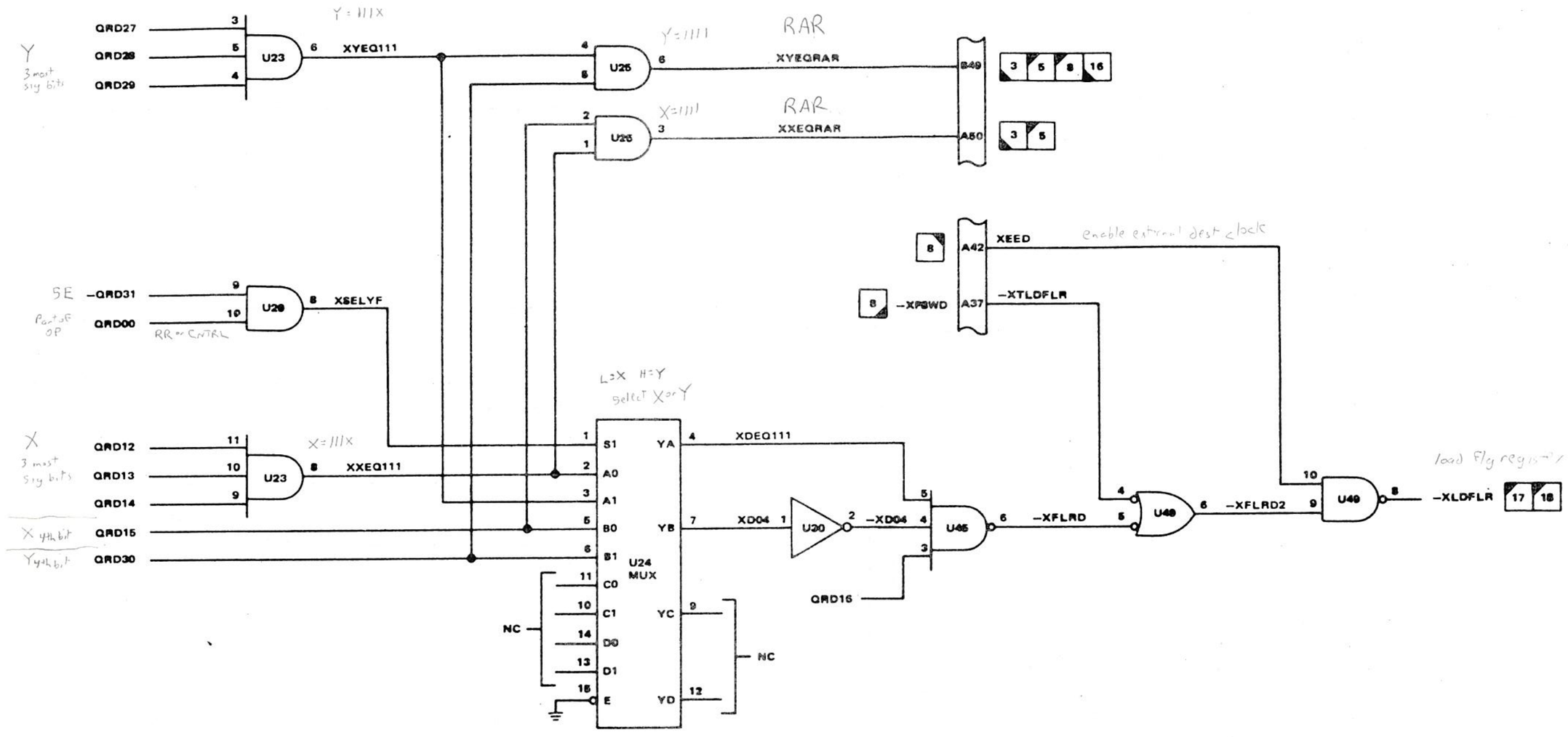


MICROPROGRAM ROM/ROM DATA REGISTER



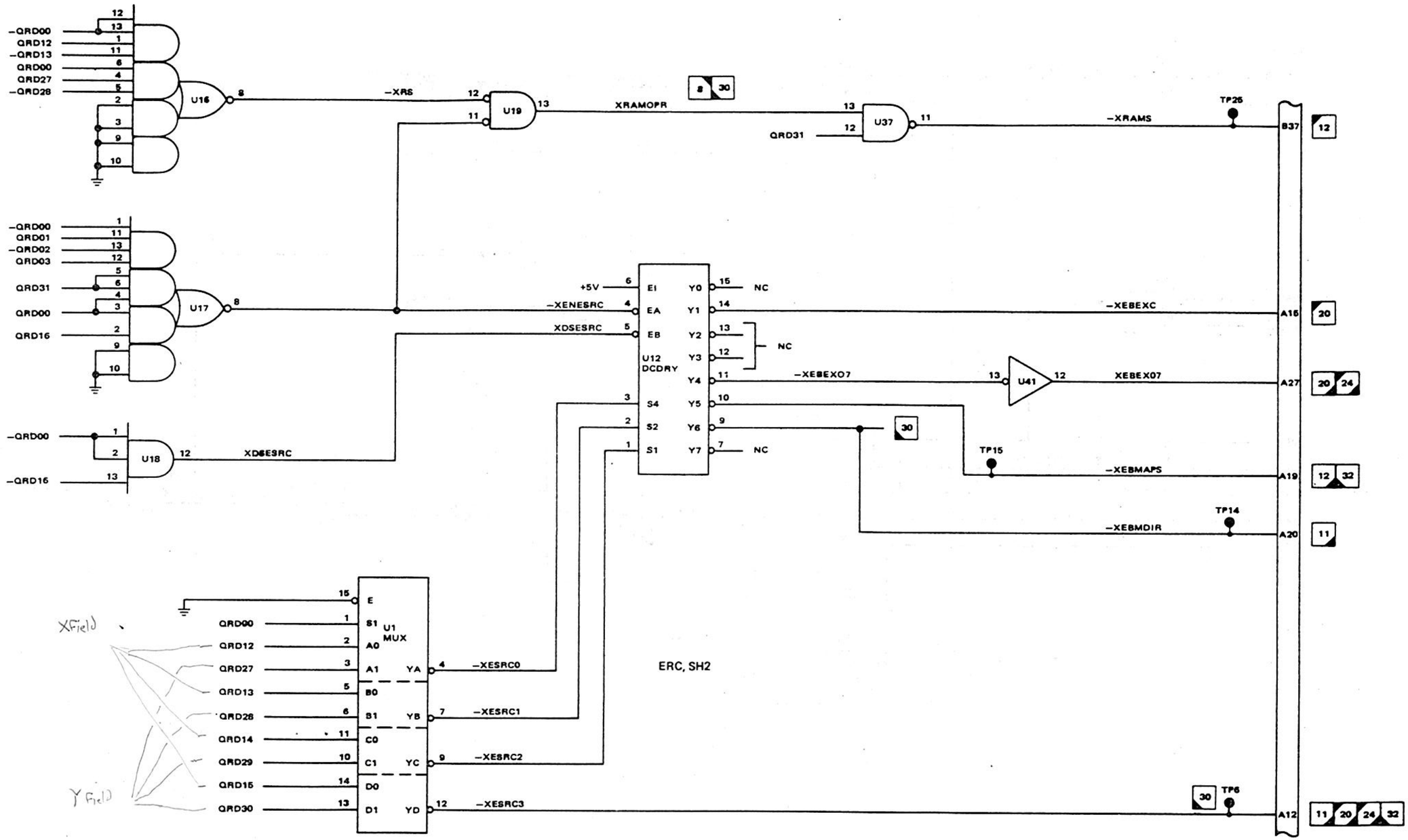
XEDSTP	-XIRD	-XMDRD	OP-CODE	MOD	QMAR15	XLDMDRU	XLDMDRL	XLDIR
1	X	X	X	X	X	0	0	0
0	1	1	X	X	X	0	0	0
0	0	X	X	X	X	0	0	1
0	1	0	BR	X	X	0	0	0
0	1	0	IO/RI/RR	010	0	1	0	0
0	1	0	IO/RI/RR	010	1	0	1	0
0	1	0	IO/RI/RR	00X	X	1	1	0
0	1	0	IO/RI/RR	011	X	1	1	0
0	1	0	IO/RI/RR	1XX	X	1	1	0
0	1	0	CTL/MUL/DIV	XXX	X	1	1	0

REGISTER CTL LOGIC
(DESTINATION DECODE)



ARB, SH 1

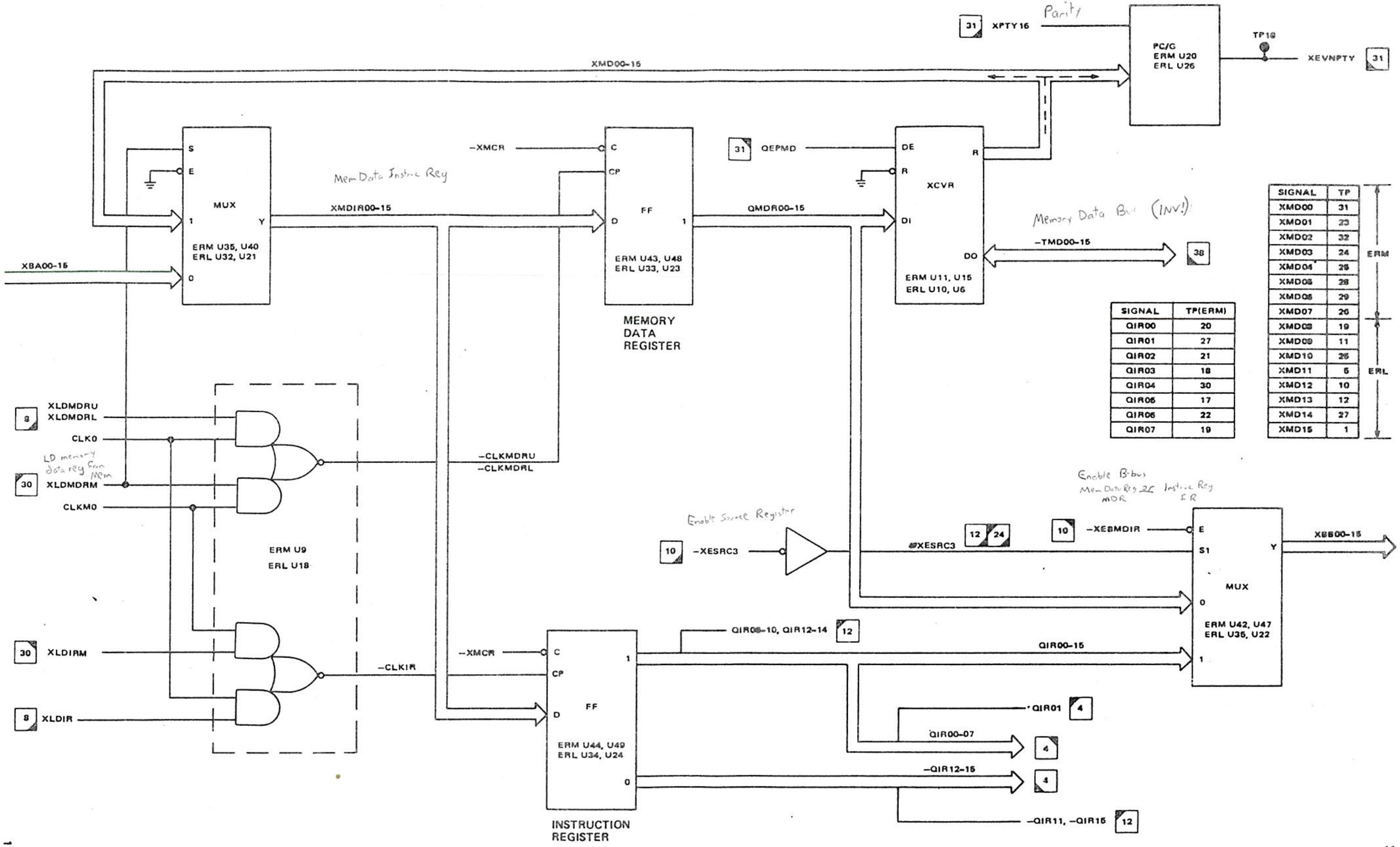
REGISTER CTL LOGIC (FLR AND RAR DECODE)



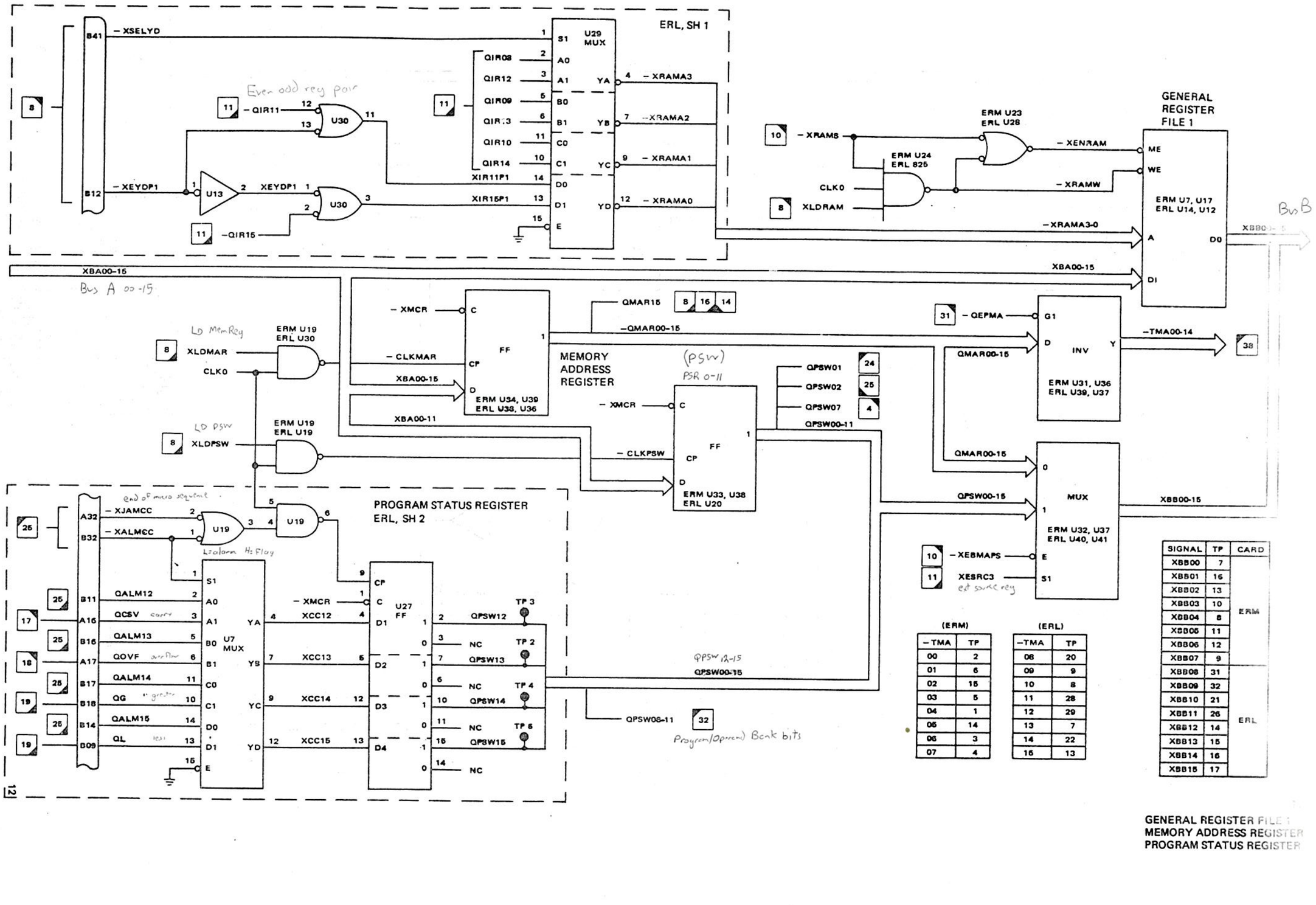
ERC, SH2

1Q

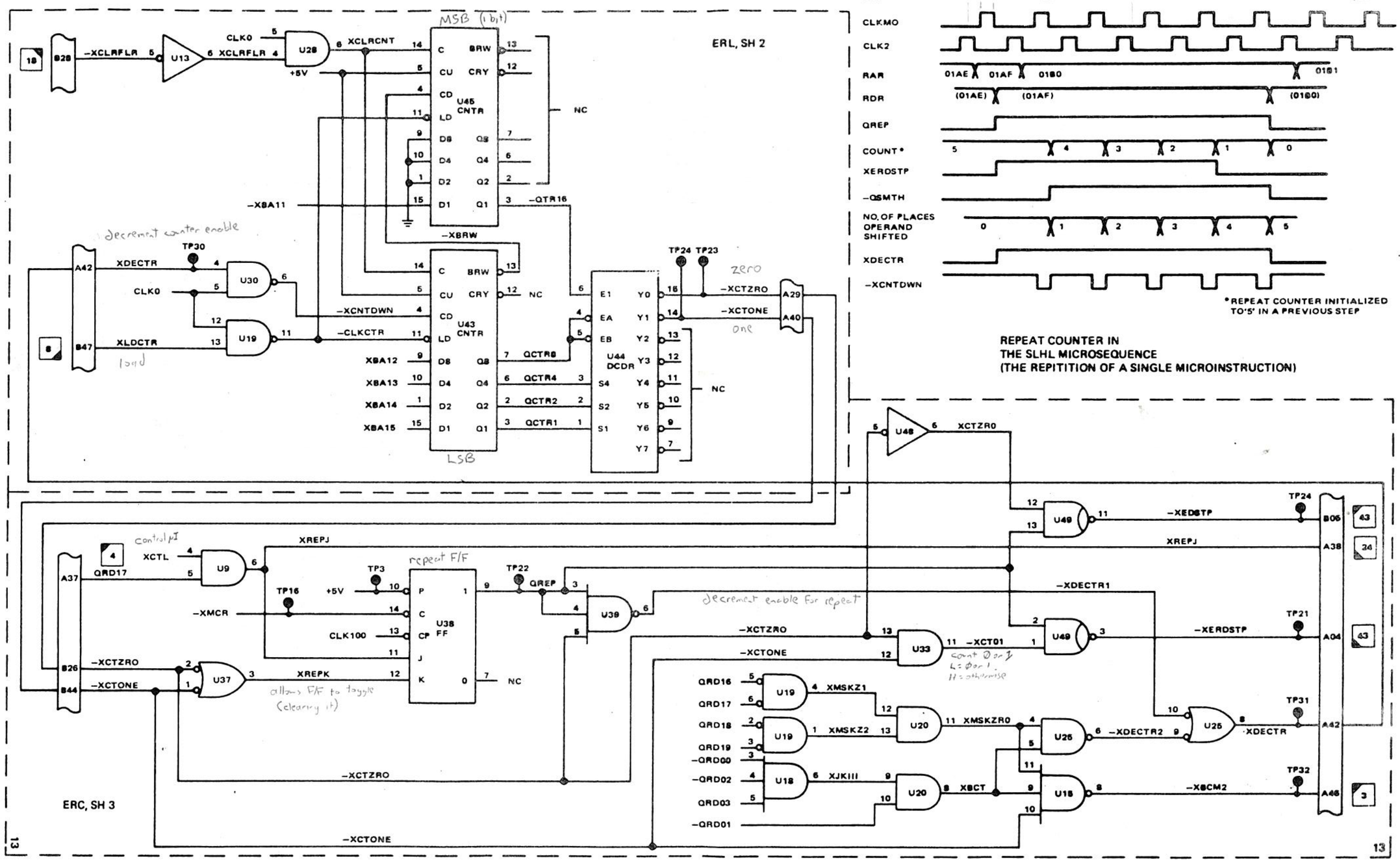
REGISTER CTL LOGIC
(SOURCE DECODE)



MEMORY DATA REGISTER
INSTRUCTION REGISTER

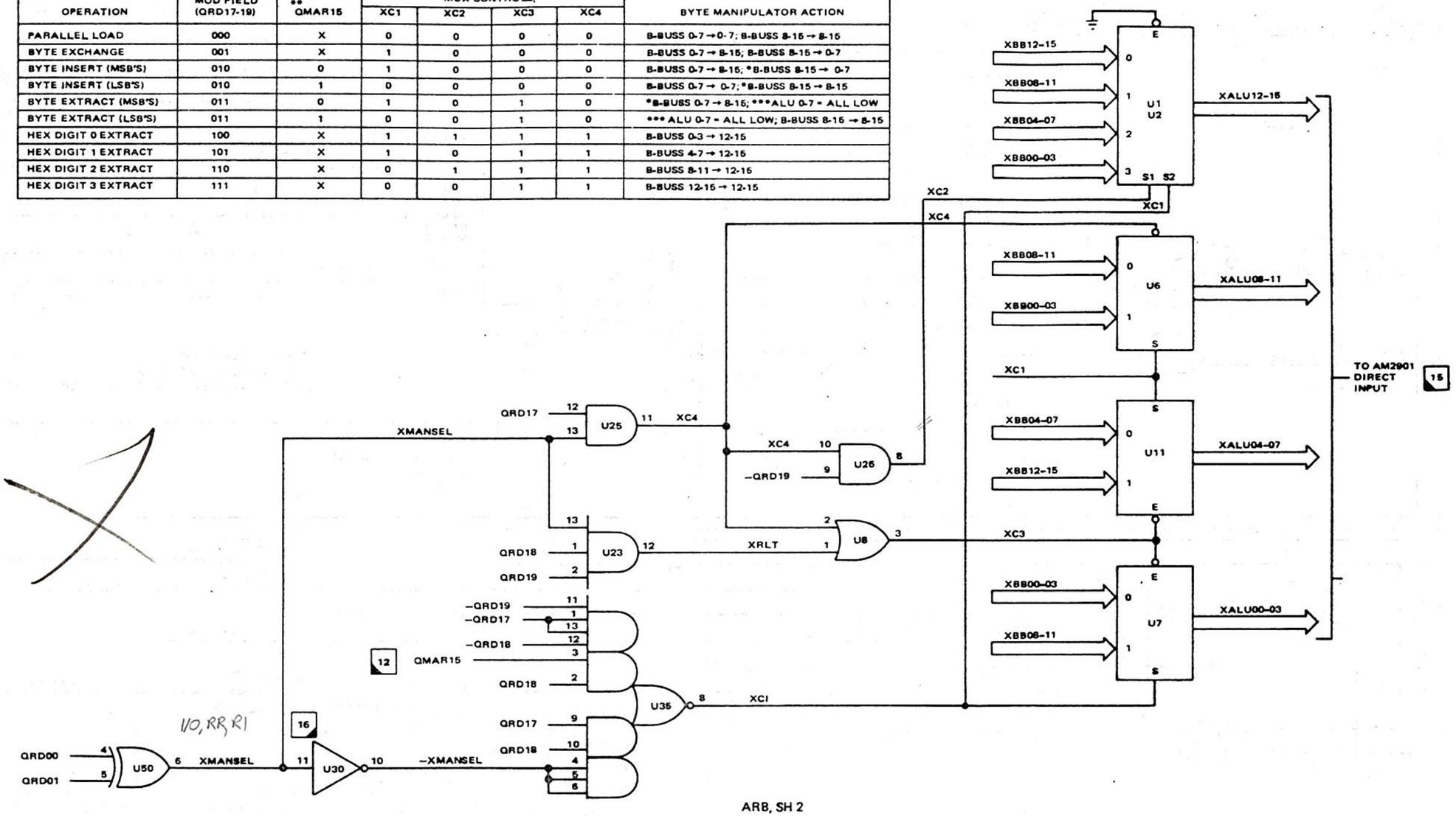


GENERAL REGISTER FILE 1
MEMORY ADDRESS REGISTER
PROGRAM STATUS REGISTER



REPEAT CTR AND CONTROL

OPERATION	MOD FIELD (QRD17-19)	** QMAR15	MUX CONTROLS				BYTE MANIPULATOR ACTION
			XC1	XC2	XC3	XC4	
PARALLEL LOAD	000	X	0	0	0	0	B-BUSS 0-7 → 0-7; B-BUSS 8-15 → 8-15
BYTE EXCHANGE	001	X	1	0	0	0	B-BUSS 0-7 → 8-15; B-BUSS 8-15 → 0-7
BYTE INSERT (MSB'S)	010	0	1	0	0	0	B-BUSS 0-7 → 8-15; *B-BUSS 8-15 → 0-7
BYTE INSERT (LSB'S)	010	1	0	0	0	0	B-BUSS 0-7 → 0-7; *B-BUSS 8-15 → 8-15
BYTE EXTRACT (MSB'S)	011	0	1	0	1	0	*B-BUSS 0-7 → 8-15; ***ALU 0-7 = ALL LOW
BYTE EXTRACT (LSB'S)	011	1	0	0	1	0	*** ALU 0-7 = ALL LOW; B-BUSS 8-15 → 8-15
HEX DIGIT 0 EXTRACT	100	X	1	1	1	1	B-BUSS 0-3 → 12-15
HEX DIGIT 1 EXTRACT	101	X	1	0	1	1	B-BUSS 4-7 → 12-15
HEX DIGIT 2 EXTRACT	110	X	0	1	1	1	B-BUSS 8-11 → 12-15
HEX DIGIT 3 EXTRACT	111	X	0	0	1	1	B-BUSS 12-15 → 12-15



ARB, SH 2

*QMAR15 IS USED TO GENERATE LOAD SIGNALS FOR BYTE INSERTION. I.E., XLDMDRU (LOAD MDR MSB'S) AND XLDMDRL (LOAD MDR LSB'S) FOR BYTE EXTRACT, BYTE MANIPULATOR PLACES BYTE → LSB'S

**QMAR15 MUST BE "0" (MAR EVEN) EXCEPT FOR BYTE OPERATIONS

***WHEN MUX DISABLED, OUTPUTS ARE "0"

BINARY POSITIONING CONTROL
ARB, SH 1

BINARY POSITIONING CONTROL
ARC, SH 1

XRD10M → U53 → –XRD10M
XMULADD, XCRYOUT → U52 → XLOGR00
XSIGN
XF3U, XOVFU → U50
QRD17, QRD18, XQ15, XCRYOUT, QCSV → U48 MUX → XR00, XQ1531
XQ1531 → A35
XR00 → A19 → XQ00
XR00, XQ08, XR08
XR15, XQ15 → B13, B24
XQ16, XR31, XQ31

U16, U46 ALU
XALUA0–3, SALUA3, QRD12–15, XALUI5–0, XRD06M, QRD09, XRD10M, QRD11
XALUD00 → XALUD07
XBA00-07
XCRYOUT, –XG00, –XG04, –XP00, XP04, XOVFU, XF3U
–CLKUALU
XCRIN04, XCRIN00
LOC=R7
File2

U26, U36 ALU
XALUA0–3, QRD12–15, XALUI5–0, XRD06M, QRD09, XRD10M, QRD11
XALUD08 → XALUD15
XBA08-15
NC, –XG12, –XG08, –XP12, –XP08, NC
–CLKLALU
XALUCIN, XCRIN08

U16, U26 U36, U46 ALU
XALUA0–3, QRD12–15, XALUI5–0, XRD06M, QRD09, XRD10M, QRD11
XBA00–15
XBB00–15
XCROUTL
–XG28, –XG24, –XG20, –XG16
–XP28, –XP24, –XP20, –XP16
XOVFLL
NC
XFEQ0L → A02
–CLKALUD
XCRYINM, XCRIN08, XCRIN04, XCRIN00

ARB, SH 1
A36, B50 → –XLRXX, –QNPT-A → U45 → –XENALU
–QRD35
Single Precision

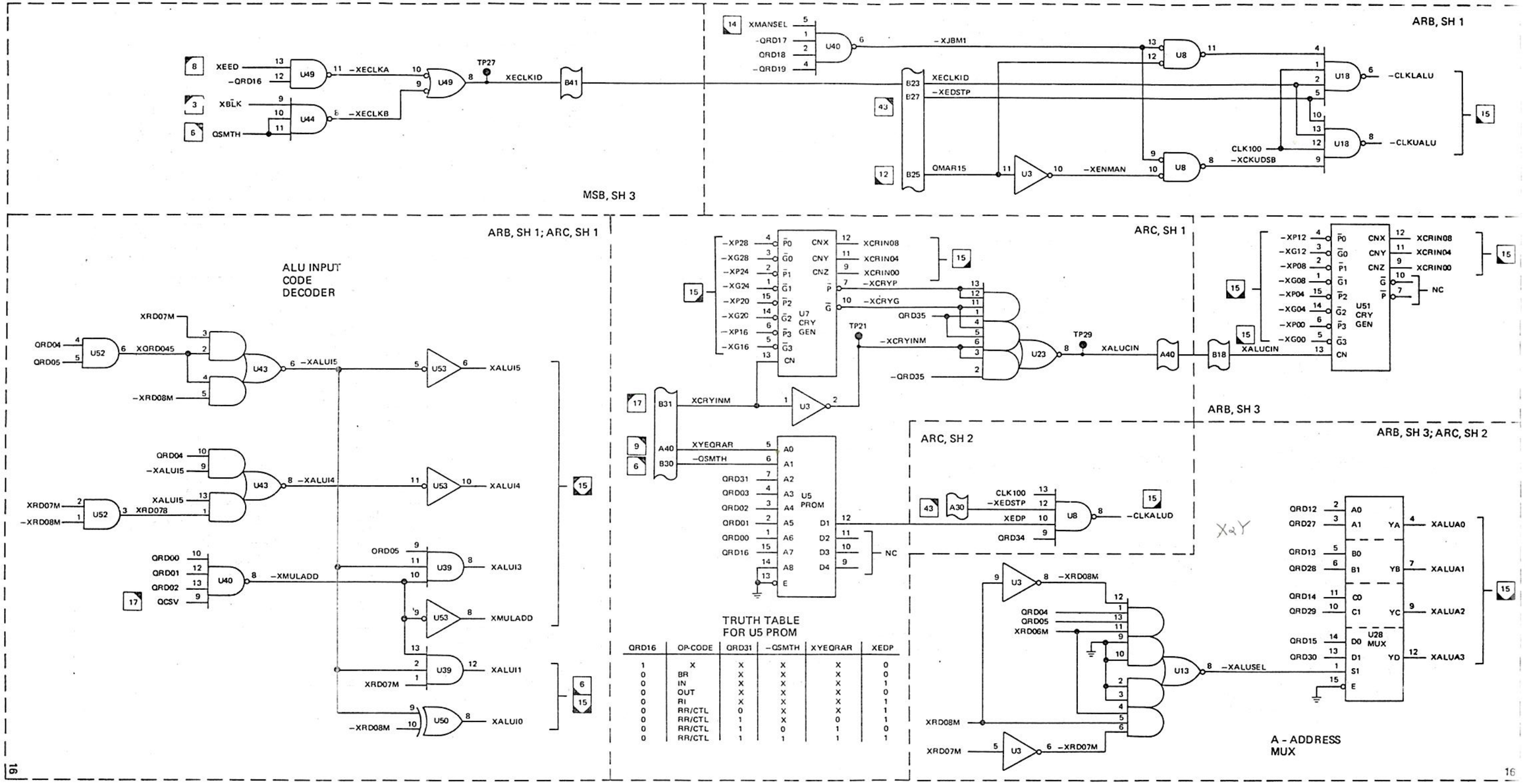
XFEQOU

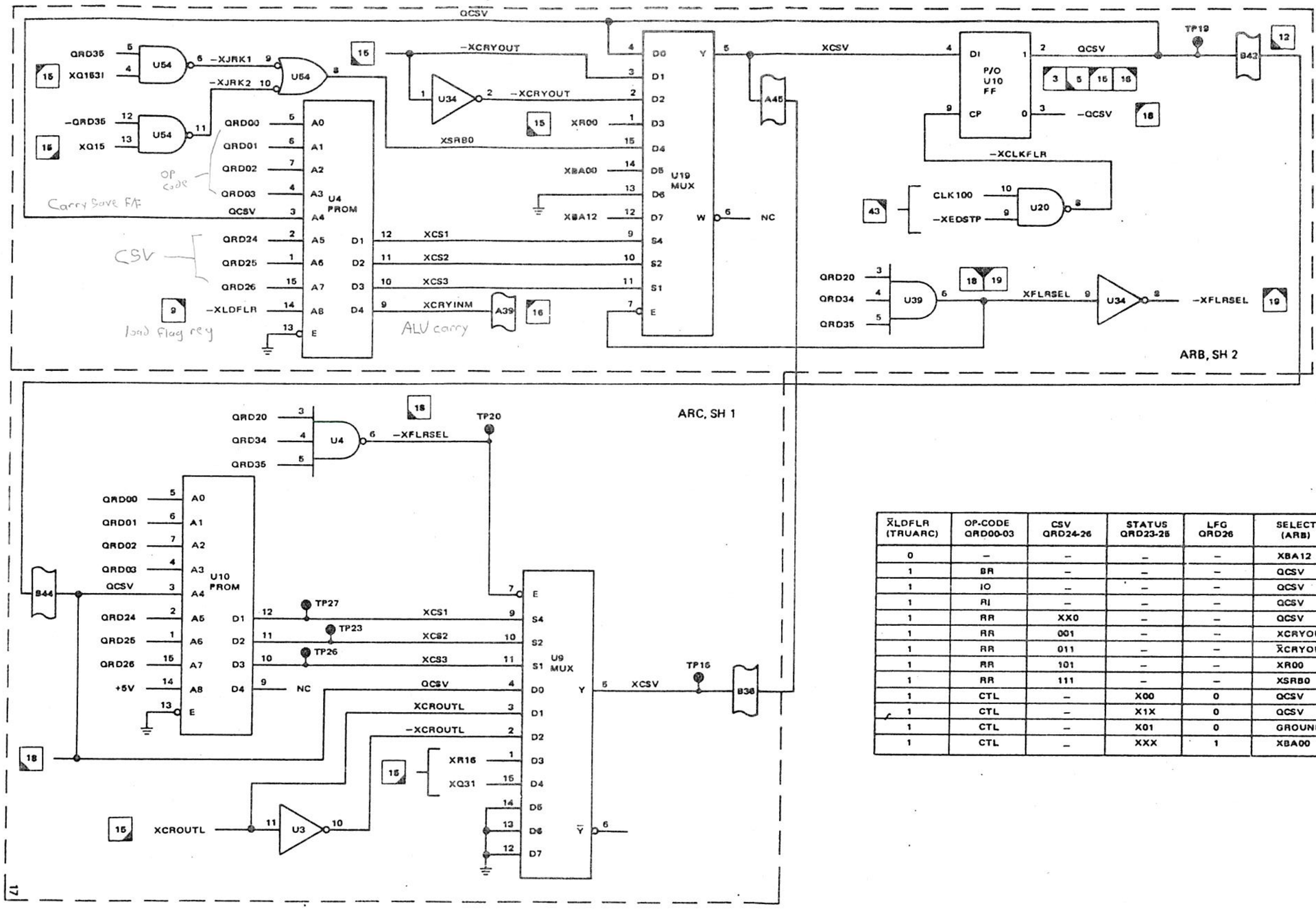
ARB, SH 3

B32, B35 → –XLRXX, –QNPT-A → U4 → –XENALUL
QRD35

ARC, SH 2

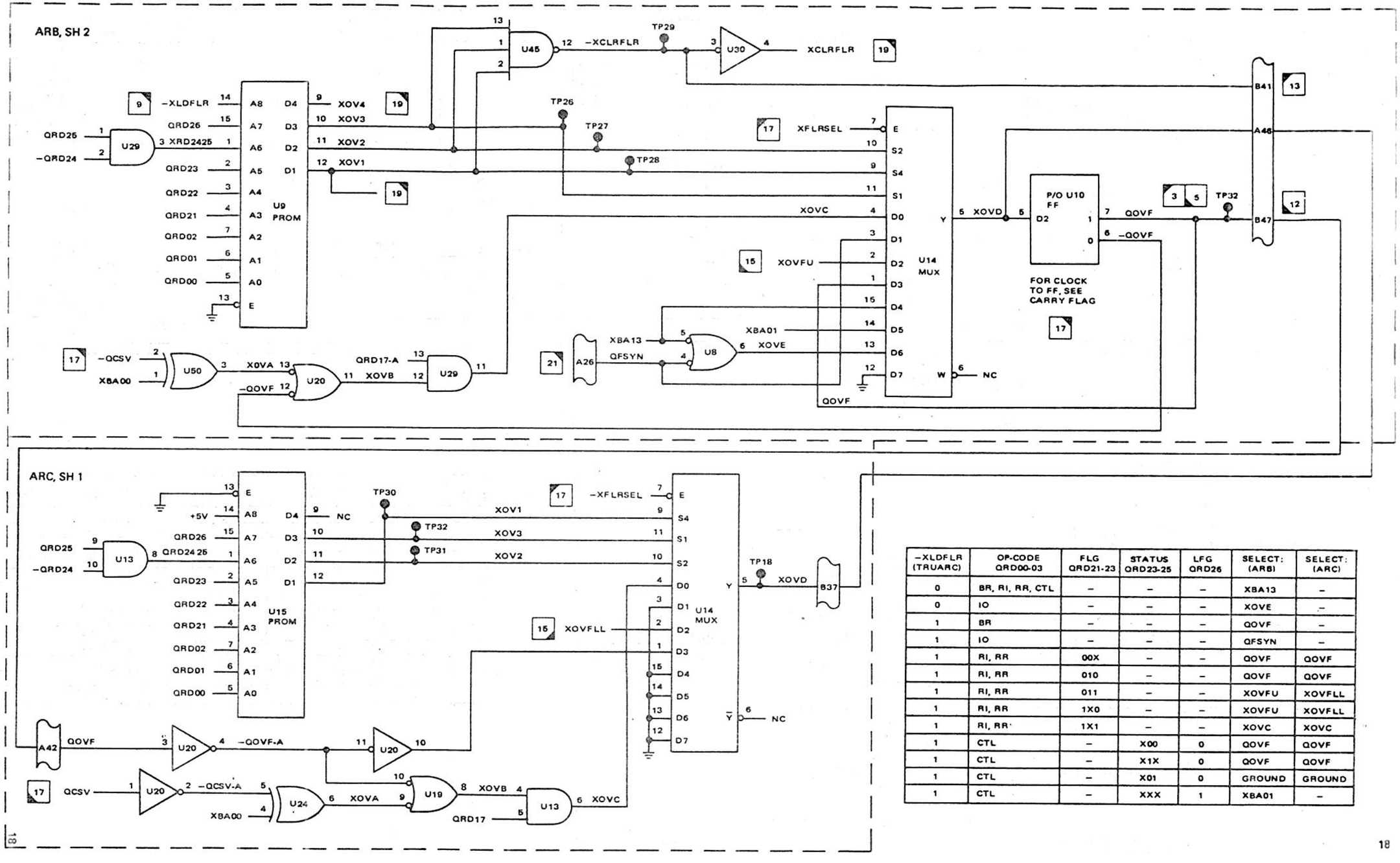
ARITHMETIC LOGIC UNIT


MSB, SH 3
ARB, SH 1
ARB, SH 1; ARC, SH 1
ARC, SH 1
ARB, SH 3
ARB, SH 3; ARC, SH 2
ARC, SH 2
ALU INPUT CODE DECODER
XEED
-QRD16
XBLK
QSMTH
-XECLKA
-XECLKB
TP27
XECLKID
XMANSEL
-QRD17
QRD18
-QRD19
-XJBM1
-XEDSTP
QMAR15
-XENMAN
CLK100
-XCKUDSB
-CLKLALU
-CLKUALU
XRD07M
QRD04
QRD05
XQRD045
-XRD08M
-XALUI5
XALUI5
-XALUI4
XALUI4
XRD078
QRD00
QRD01
QRD02
QCSV
-XMULADD
XMULADD
XALUI3
XALUI1
XALUI0
-XP28
-XG28
-XP24
-XG24
-XP20
-XG20
-XP16
-XG16
XCRIN08
XCRIN04
XCRIN00
-XCRYP
-XCRYG
-XCRYINM
QRD35
-QRD35
TP21
TP29
XALUCIN
XCRYINM
XYEQRAR
-QSMTH
QRD31
QRD03
QRD02
QRD01
QRD00
QRD16
NC
TRUTH TABLE FOR U5 PROM
QRD16 | OP-CODE | QRD31 | -QSMTH | XYEQRAR | XEDP
1 | X | X | X | X | 0
0 | BR | X | X | X | 0
0 | IN | X | X | X | 1
0 | OUT | X | X | X | 0
0 | RI | X | X | X | 1
0 | RR/CTL | 0 | X | X | 1
0 | RR/CTL | 1 | X | 0 | 1
0 | RR/CTL | 1 | 0 | 1 | 0
0 | RR/CTL | 1 | 1 | 1 | 1
-CLKALUD
XRD08M
XRD07M
-XALUSEL
A - ADDRESS MUX
XALUA0
XALUA1
XALUA2
XALUA3
QRD12
QRD27
QRD13
QRD28
QRD14
QRD29
QRD15
QRD30
NC

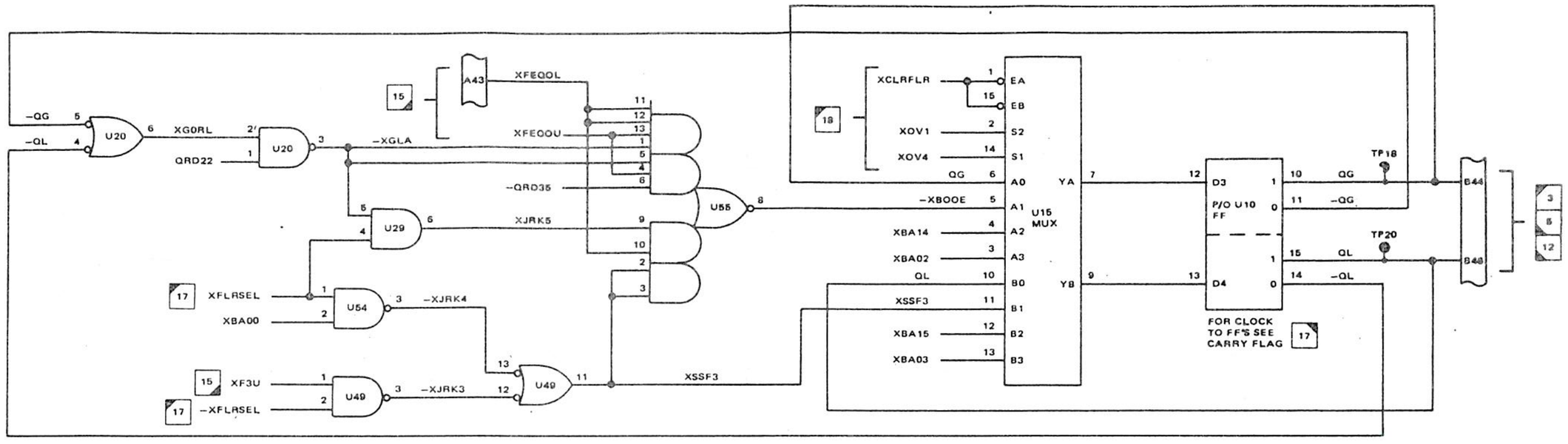


OP CODE	QCSV	XCRYINM
0	X	0
1	X	0
2	X	0
3	X	0
4	X	0
5	X	0
6	X	0
7	X	1
8	X	0
9	X	1
A	0	0
	1	1
B	0	1
	1	0
C	X	0
D	X	1
E	0	1
	1	0
F	0	1
	1	0

$\overline{X}$LDFLR (TRUARC)	OP-CODE QRD00-03	CSV QRD24-26	STATUS QRD23-25	LFG QRD26	SELECT: (ARB)	SELECT: (ARC)
0	–	–	–	–	XBA12	–
1	BR	–	–	–	QCSV	–
1	IO	–	–	–	QCSV	–
1	RI	–	–	–	QCSV	QCSV
1	RR	XX0	–	–	QCSV	QCSV
1	RR	001	–	–	XCRYOUT	XCROUTL
1	RR	011	–	–	$\overline{X}$CRYOUT	$\overline{X}$CROUTL
1	RR	101	–	–	XR00	XR16
1	RR	111	–	–	XSRB0	XQ31
1	CTL	–	X00	0	QCSV	QCSV
1	CTL	–	X1X	0	QCSV	QCSV
1	CTL	–	X01	0	GROUND	GROUND
1	CTL	–	XXX	1	XBA00	–

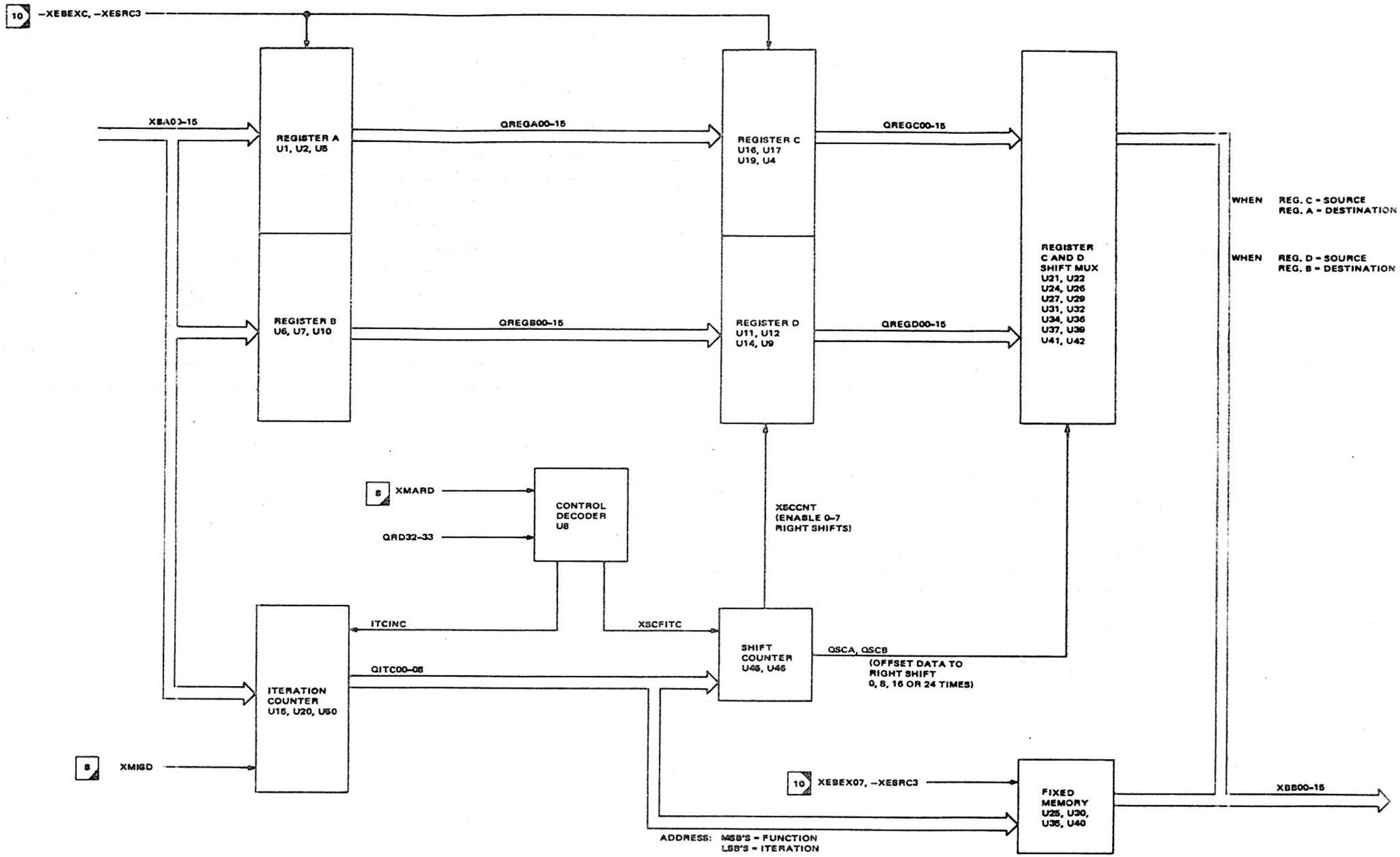


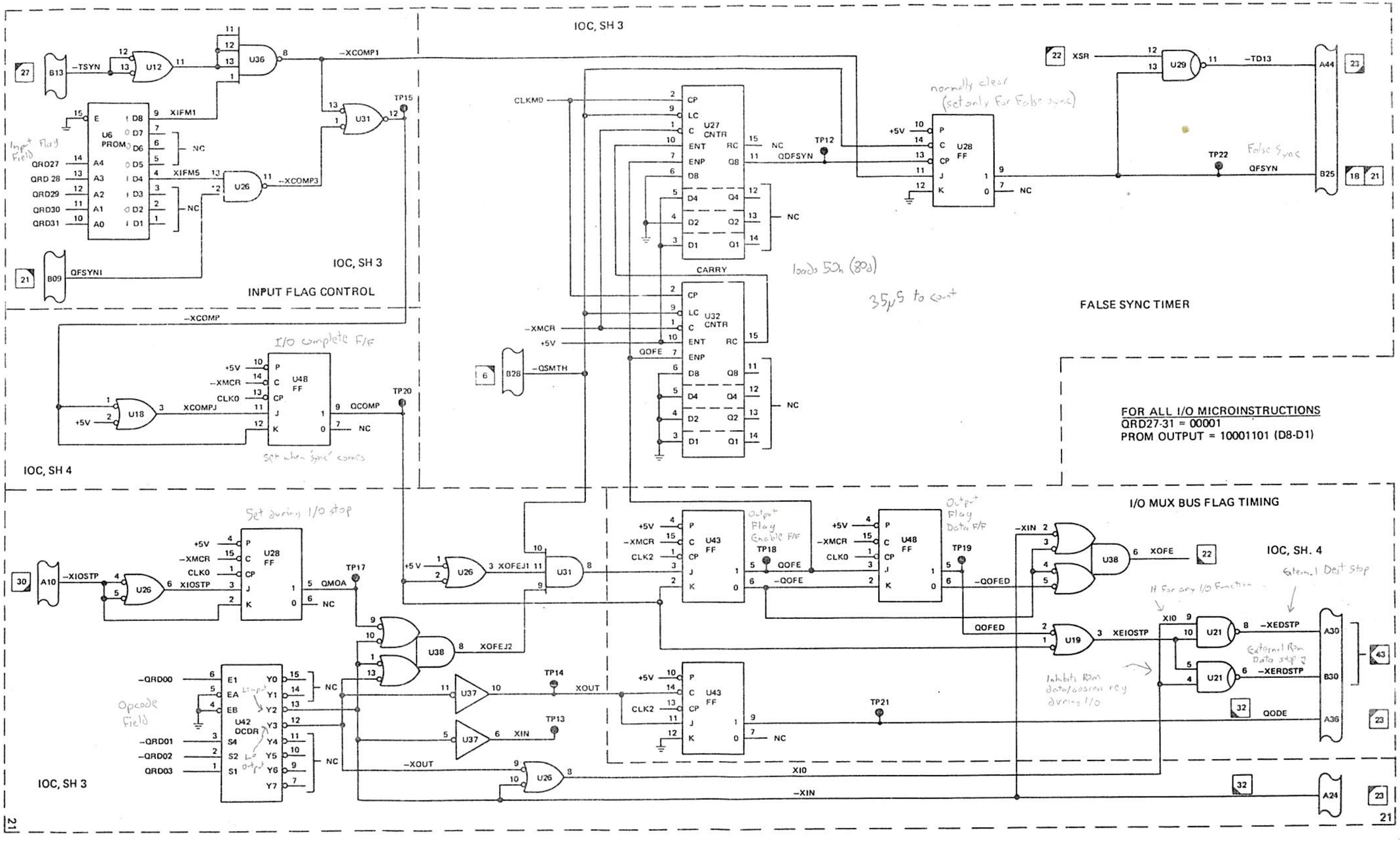
-XLDFLR (TRUARC)	OP-CODE QRD00-03	FLG QRD21-23	STATUS QRD23-25	LFG QRD26	SELECT: (ARB)	SELECT: (ARC)
0	BR, RI, RR, CTL	–	–	–	XBA13	–
0	IO	–	–	–	XOVE	–
1	BR	–	–	–	QOVF	–
1	IO	–	–	–	QFSYN	–
1	RI, RR	00X	–	–	QOVF	QOVF
1	RI, RR	010	–	–	QOVF	QOVF
1	RI, RR	011	–	–	XOVFU	XOVFLL
1	RI, RR	1X0	–	–	XOVFU	XOVFLL
1	RI, RR	1X1	–	–	XOVC	XOVC
1	CTL	–	X00	0	QOVF	QOVF
1	CTL	–	X1X	0	QOVF	QOVF
1	CTL	–	X01	0	GROUND	GROUND
1	CTL	–	XXX	1	XBA01	–



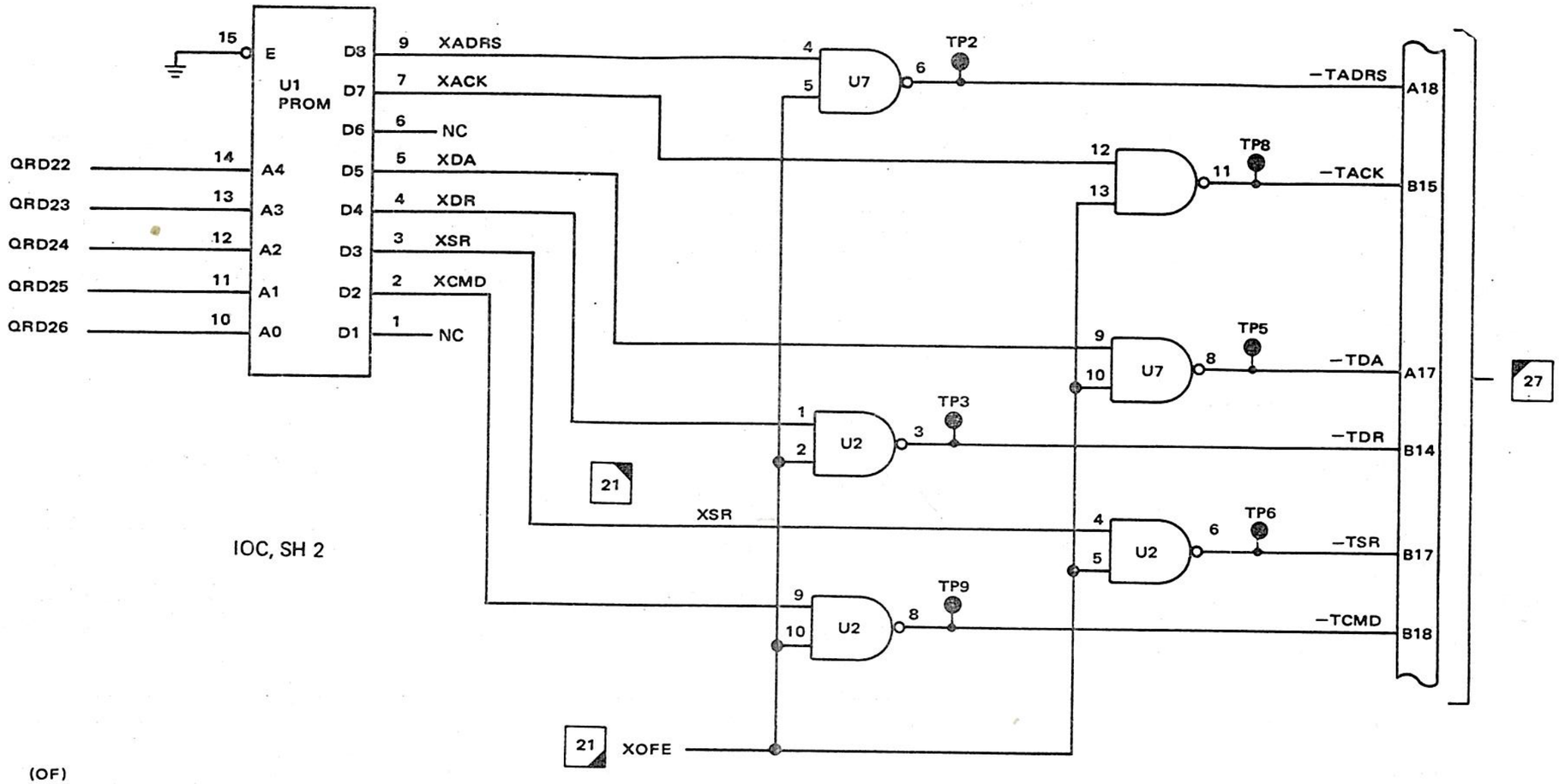
-XLDFLR	OP-CODE QRD60-03	FLG QRD21-23	STATUS QRD23-25	LFG QRD26	XCLRFLR	SELECTION
0	–	–	–	–	0	XBA14/XBA15
1	BR	–	–	–	0	QG/QL
1	IO	–	–	–	0	QG/QL
1	RI/RR	000	–	–	0	QG/QL
1	RI/RR	001	–	–	0	-XB00E/XSSF3
1	RI/RR	01X	–	–	0	-XB00E/XBSF3
1	RI/RR	10X	–	–	0	-XB00E/X8SF3
1	RI/RR	11X	–	–	0	QG/QL
1	CTL	–	X00	0	0	QG/QL
1	CTL	–	X1X	0	0	QG/QL
1	CTL	–	X01	0	1	–
1	CTL	–	XXX	1	0	XBA02/XBA03

G AND L FLAGS
AND CONTROL
ARB, SH 2


10 –XEBEXC, –XESRC3
XBA00–15
REGISTER A
U1, U2, U5
QREGA00–15
REGISTER C
U16, U17
U19, U4
QREGC00–15
REGISTER
C AND D
SHIFT MUX
U21, U22
U24, U26
U27, U29
U31, U32
U34, U36
U37, U39
U41, U42
WHEN REG. C = SOURCE
REG. A = DESTINATION
WHEN REG. D = SOURCE
REG. B = DESTINATION
REGISTER B
U6, U7, U10
QREGB00–15
REGISTER D
U11, U12
U14, U9
QREGD00–15
8 XMARD
QRD32–33
CONTROL
DECODER
U8
XSCCNT
(ENABLE 0–7
RIGHT SHIFTS)
ITCINC
XSCFITC
SHIFT
COUNTER
U43, U46
QSCA, QSCB
(OFFSET DATA TO
RIGHT SHIFT
0, 8, 16 OR 24 TIMES)
ITERATION
COUNTER
U15, U20, U50
QITC00–05
8 XMIGD
10 XEBEX07, –XESRC3
FIXED
MEMORY
U25, U30,
U35, U40
XBB00–15
ADDRESS: MSB'S = FUNCTION
LSB'S = ITERATION



I/O MUX BUS AND FLAG TIMING CONTROL



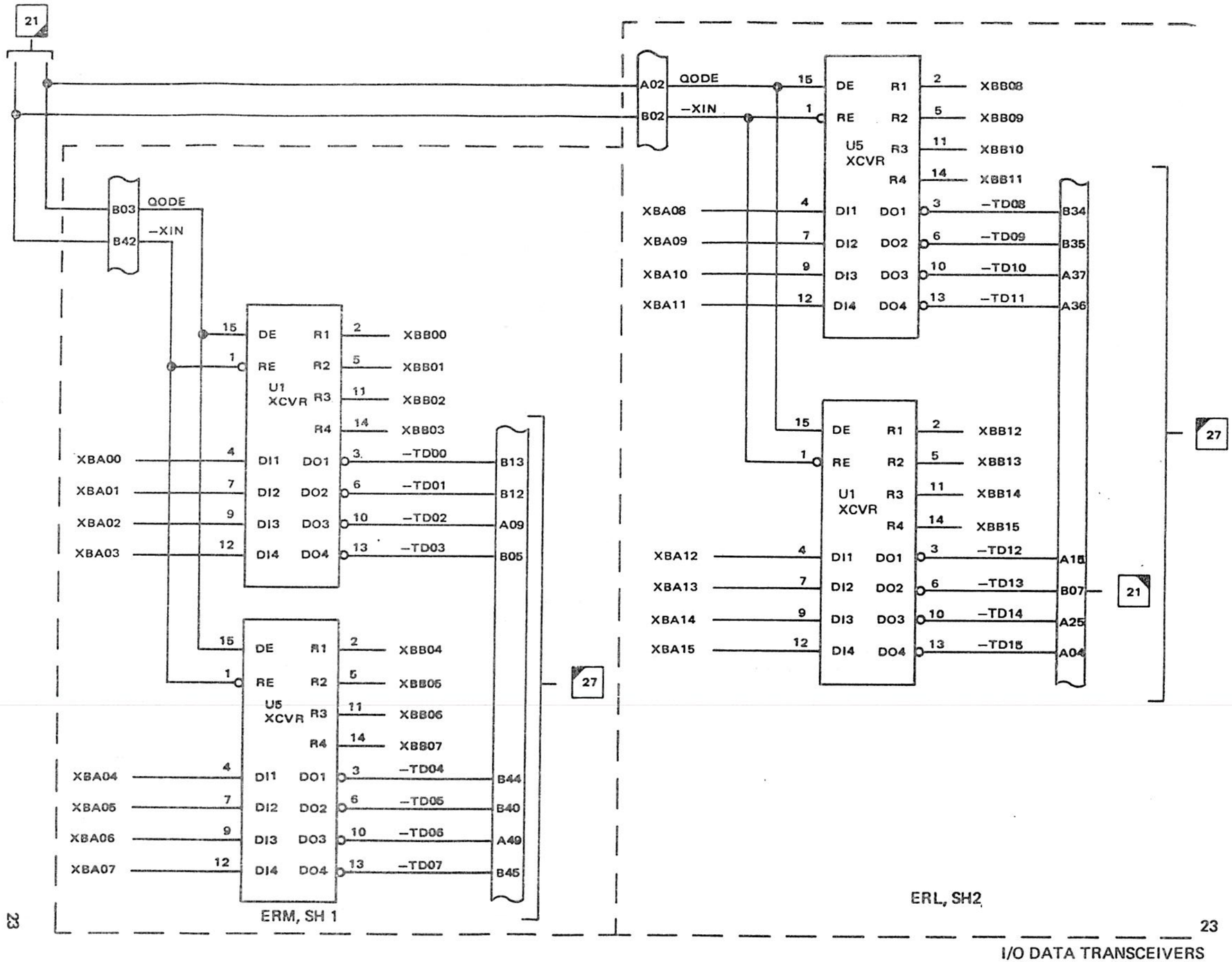
IOC, SH 2

(OF)

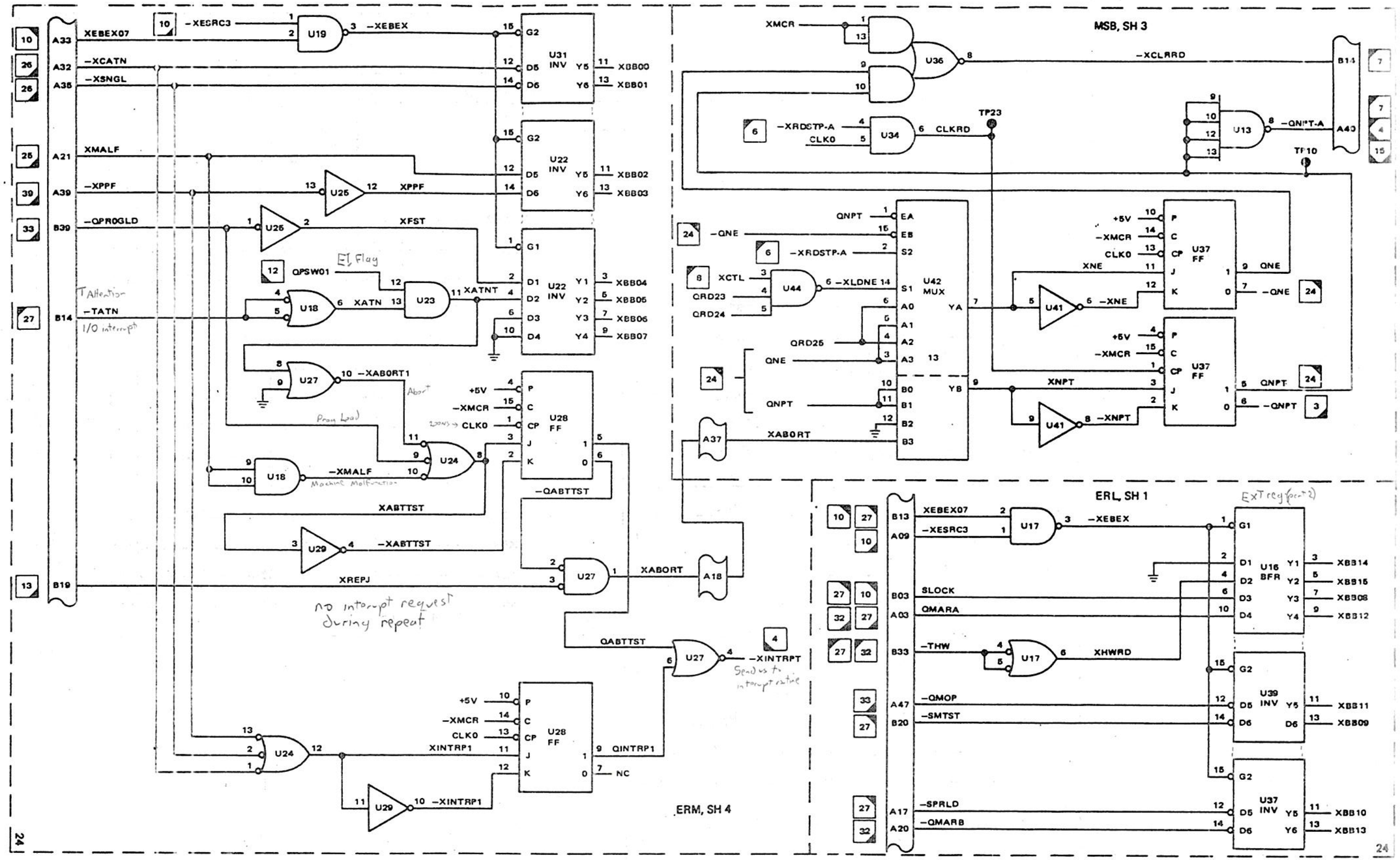
QRD22-26	XADRS	XACK	XDA	XDR	XSR	XCMD
00001	1	0	0	0	0	0
00010	0	0	0	0	0	1
00011	0	0	1	0	0	0
00100	0	0	0	1	0	0
00101	0	1	0	0	0	0
00111	0	0	0	0	1	0

OUTPUT FLAG CONTROL

22

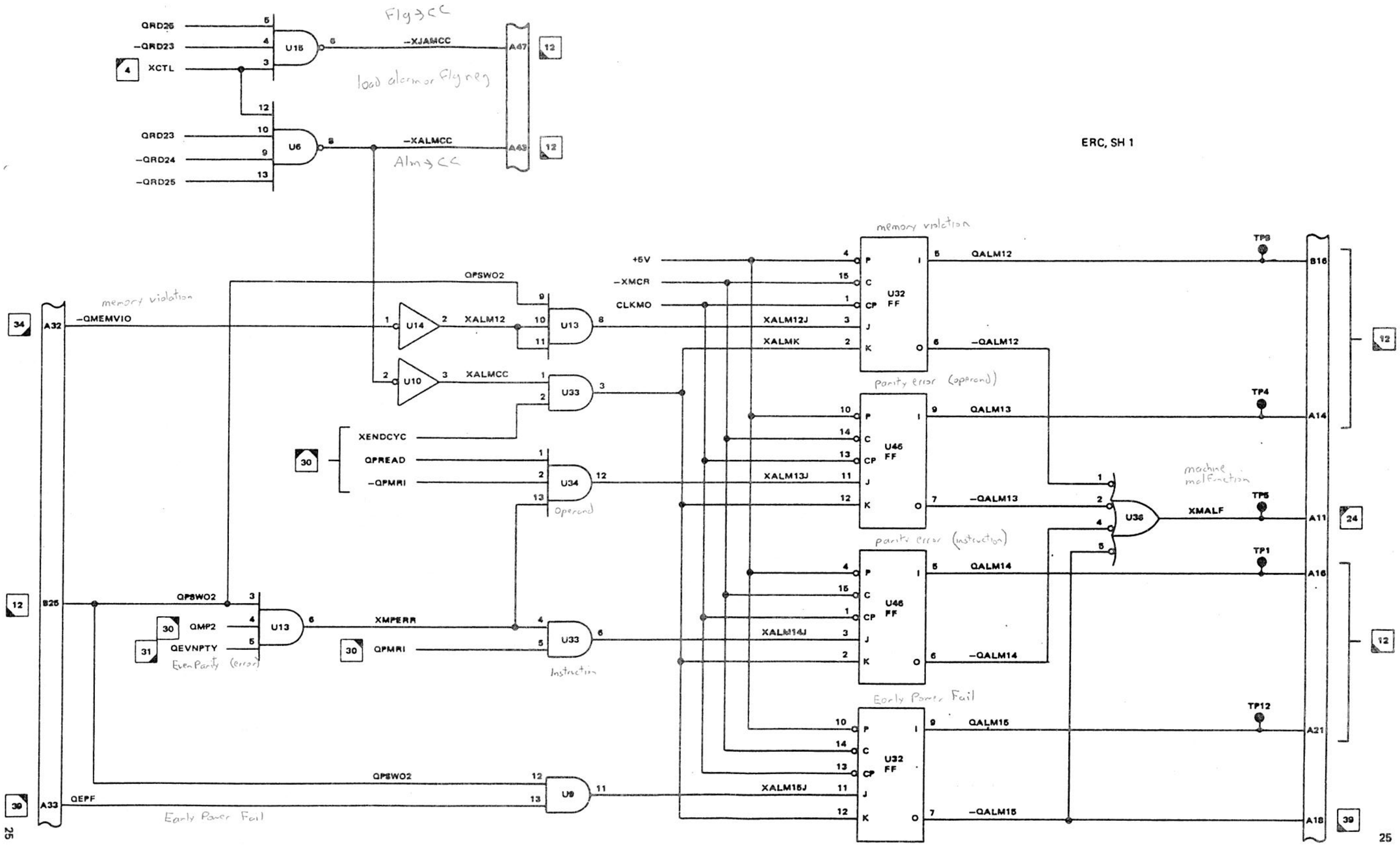

21
A02
B02
QODE
-XIN
B03
B42
QODE
-XIN
U1 XCVR
DE
RE
R1
R2
R3
R4
DI1
DI2
DI3
DI4
DO1
DO2
DO3
DO4
XBB00
XBB01
XBB02
XBB03
XBA00
XBA01
XBA02
XBA03
-TD00
-TD01
-TD02
-TD03
B13
B12
A09
B05
U5 XCVR
XBB04
XBB05
XBB06
XBB07
XBA04
XBA05
XBA06
XBA07
-TD04
-TD05
-TD06
-TD07
B44
B40
A49
B45
27
ERM, SH 1
U5 XCVR
XBB08
XBB09
XBB10
XBB11
XBA08
XBA09
XBA10
XBA11
-TD08
-TD09
-TD10
-TD11
B34
B35
A37
A36
U1 XCVR
XBB12
XBB13
XBB14
XBB15
XBA12
XBA13
XBA14
XBA15
-TD12
-TD13
-TD14
-TD15
A15
B07
A25
A04
21
27
ERL, SH2
23
23
I/O DATA TRANSCEIVERS

Ext Interrupt (KD9-50x2 pg 4-21)
EXT req part 1 (U31,22,16,37,27)

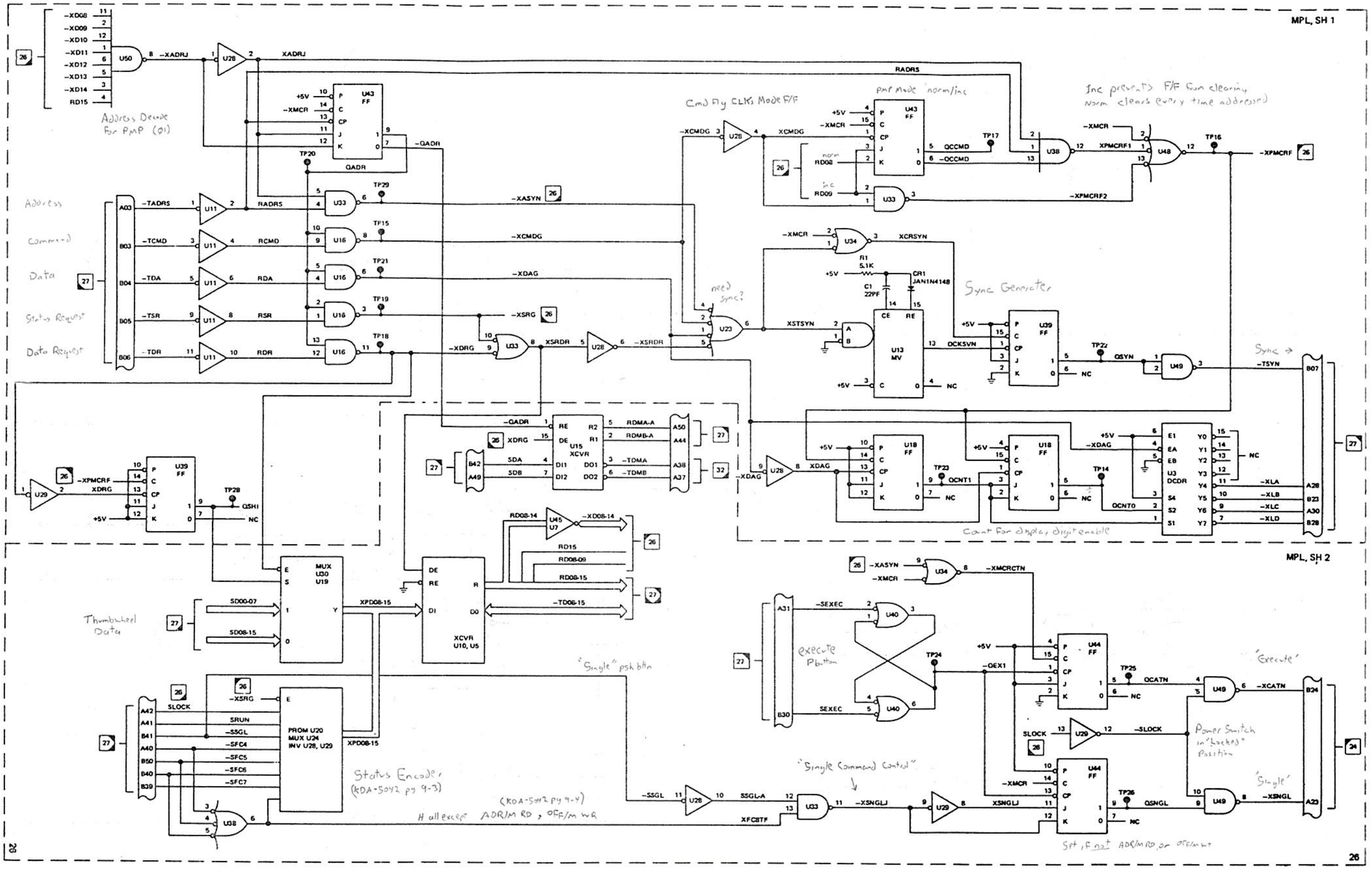


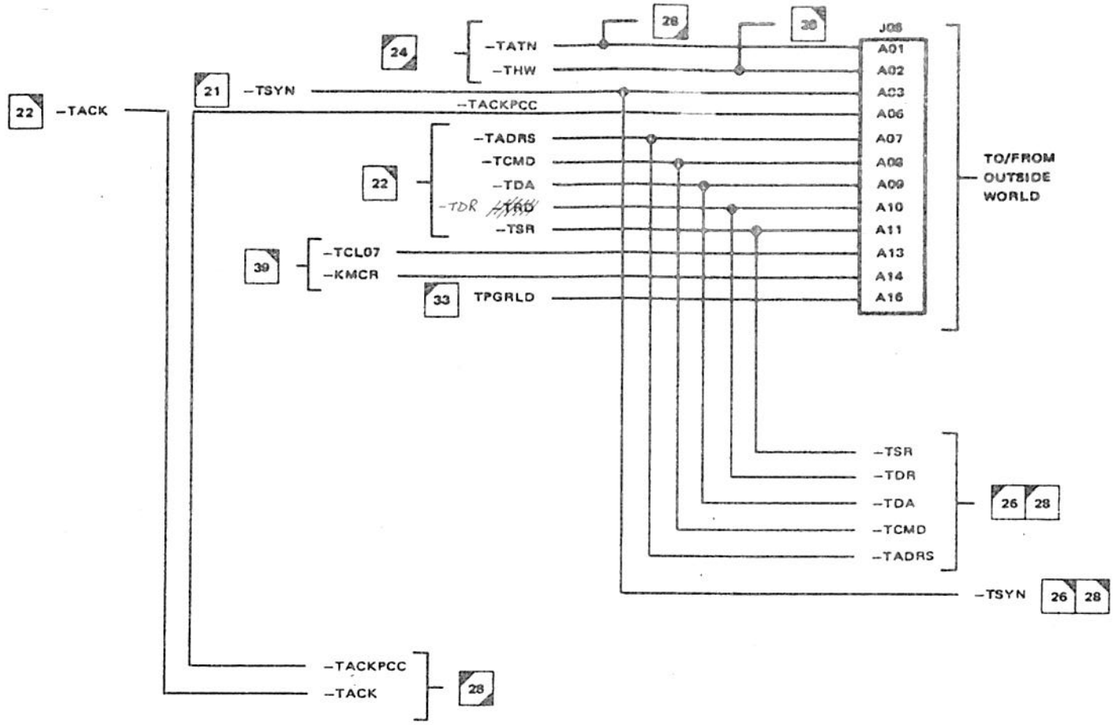
INTERRUPT LOGIC CONTROL

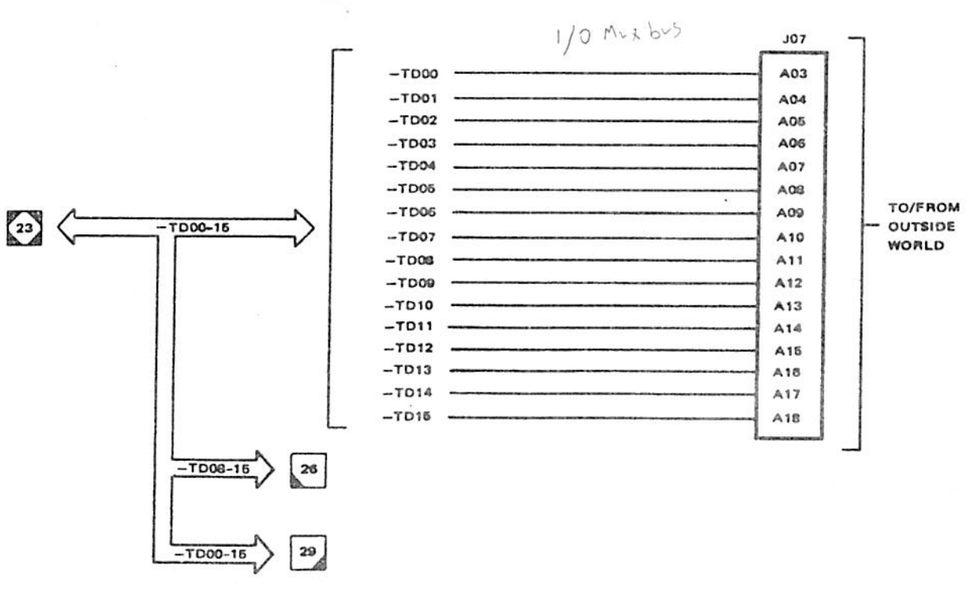
ERC, SH 1

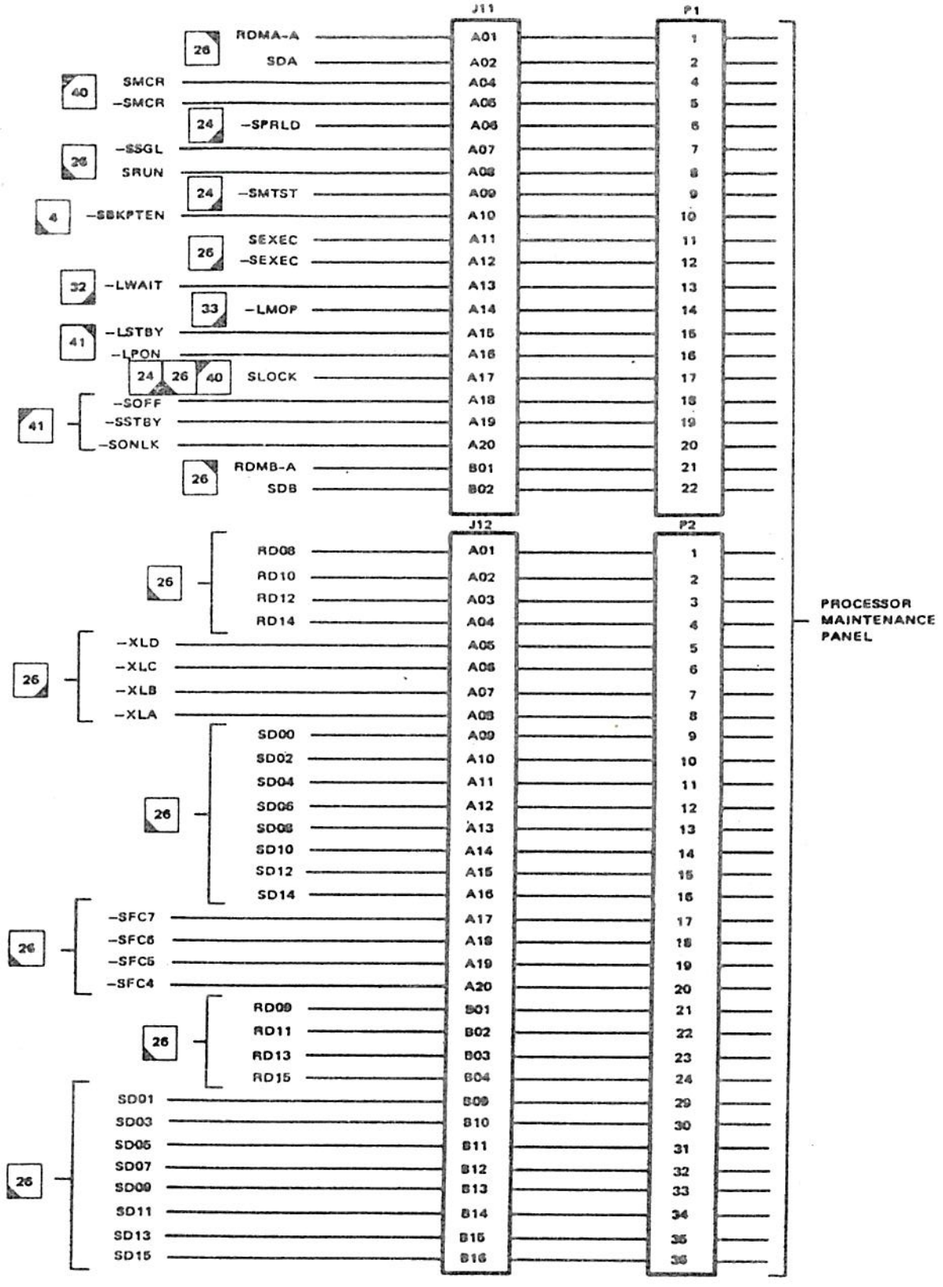


ALARM REG.


-XD08
-XD09
-XD10
-XD11
-XD12
-XD13
-XD14
RD15
U50
-XADRJ
U28
XADRJ
RADRS
Address Decode For PMP (Φ1)
U43 FF
+5V
-XMCR
QADR
-QADR
TP20
Cmd Fly CLKs Mode F/F
PMP Mode 'norm/inc
-XCMDG
XCMDG
RD08
RD09
QCCMD
-QCCMD
TP17
U38
Inc prevents F/F from clearing
Norm clears every time addressed
XPMCRF1
U48
TP16
-XPMCRF
-XPMCRF2
Address
Command
Data
Status Request
Data Request
A03
B03
B04
B05
B06
-TADRS
-TCMD
-TDA
-TSR
-TDR
U11
RCMD
RDA
RSR
RDR
TP29
TP15
TP21
TP19
TP18
U16
-XASYN
-XCMDG
-XDAG
-XSRG
-XDRG
U33
XSRDR
-XSRDR
need sync?
U23
U34
XCRSYN
R1 5.1K
C1 22PF
CR1 JAN1N4148
Sync Generator
XSTSYN
U13 MV
DCKSYN
U39 FF
TP22
QSYN
U49
Sync →
-TSYN
B07
-XADRJ
U29
-XPMCRF
XDRG
QSHI
TP28
NC
U15 XCVR
RDMA-A
RDMB-A
-TDMA
-TDMB
SDA
SDB
B42
A49
A50
A44
A38
A37
U18 FF
OCNT1
OCNT0
TP23
TP14
U3 DCDR
-XLA
-XLB
-XLC
-XLD
A28
B23
A30
B28
Count for display digit enable
Disp 1
-XLD
-XLC
Disp 2
-XLB
-XLA
MPL, SH 2
MUX U30 U19
SD00-07
SD08-15
XPD08-15
Thumbwheel Data
XCVR U10, U5
RD08-14
U45 U7
-XD08-14
RD15
RD08-09
RD08-15
-TD08-15
PROM U20 MUX U24 INV U28, U29
SLOCK
SRUN
-SSGL
-SFC4
-SFC5
-SFC6
-SFC7
A42
A41
B41
A40
B50
B40
B39
Status Encoder (KDA-5042 pg 9-3)
U38
-SSGL
SSGL-A
XFC8TF
U33
-XSNGLJ
XSNGLJ
U29
(KDA-5042 pg 9-4)
H all except ADR/M RD, OFF/M WR
-XMCRCTN
U34
-SEXEC
SEXEC
A31
B30
U40
execute Pbutton
TP24
-OEX1
U44 FF
TP25
OCATN
U49
-XCATN
B24
'Execute'
SLOCK
U29
-SLOCK
Power Switch in "locked" Position
TP26
QSNGL
'Single'
-XSNGL
A23
"Single" psh btn
"Single (command) Control"
Set, if not ADR/M RD or OFF/M WR







I/O MUX BUS FUNCTIONAL WIRE DIAGRAM

PCC, SH 1

PCC, SH2

PCC, SH3

PCC, SH 2

COUNT TIMING

ETC REGISTER

40h selects PCC thru U25

adrs F/F

Overflow or Time Out

I/O int F/F

Load ETC

LD F/F

ETC int enbl F/F

Arm

time out

set time out F/F

25nS

÷ 125

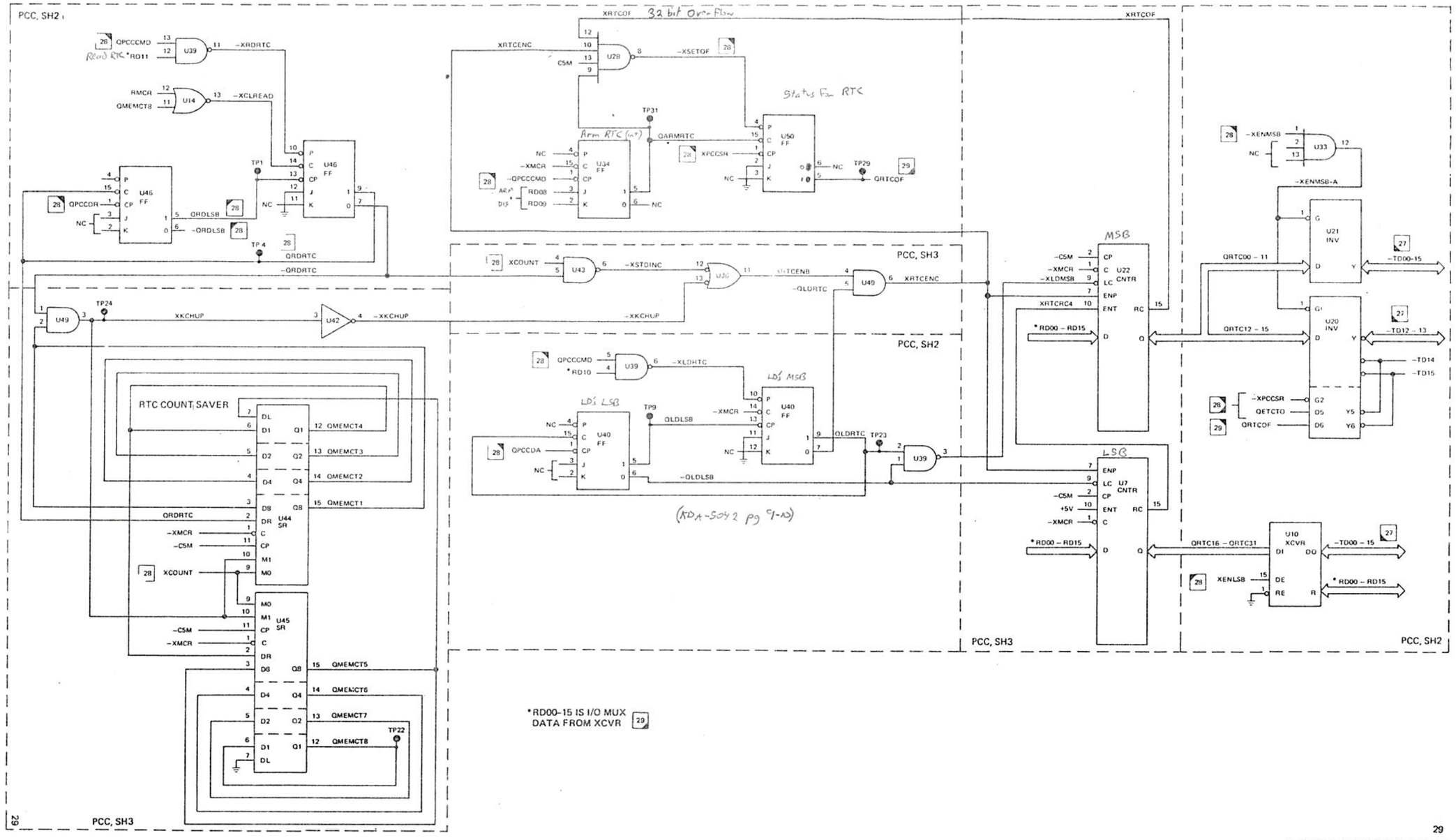
U4,U2,U15

C5M = CLKM0

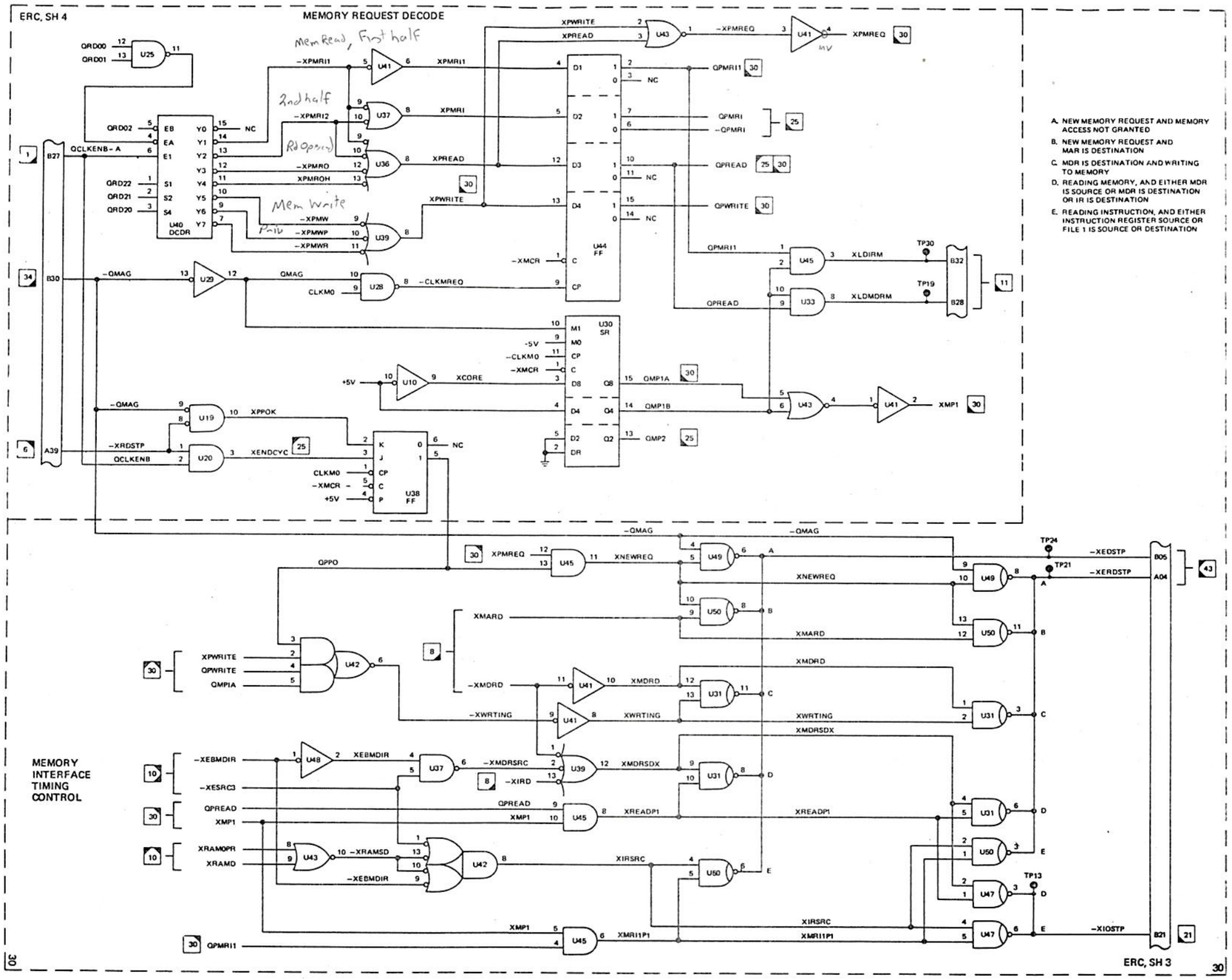
CNTR U27, U29 U26, U30

*RD00-15 IS I/O MUX DATA FROM XCVR 29

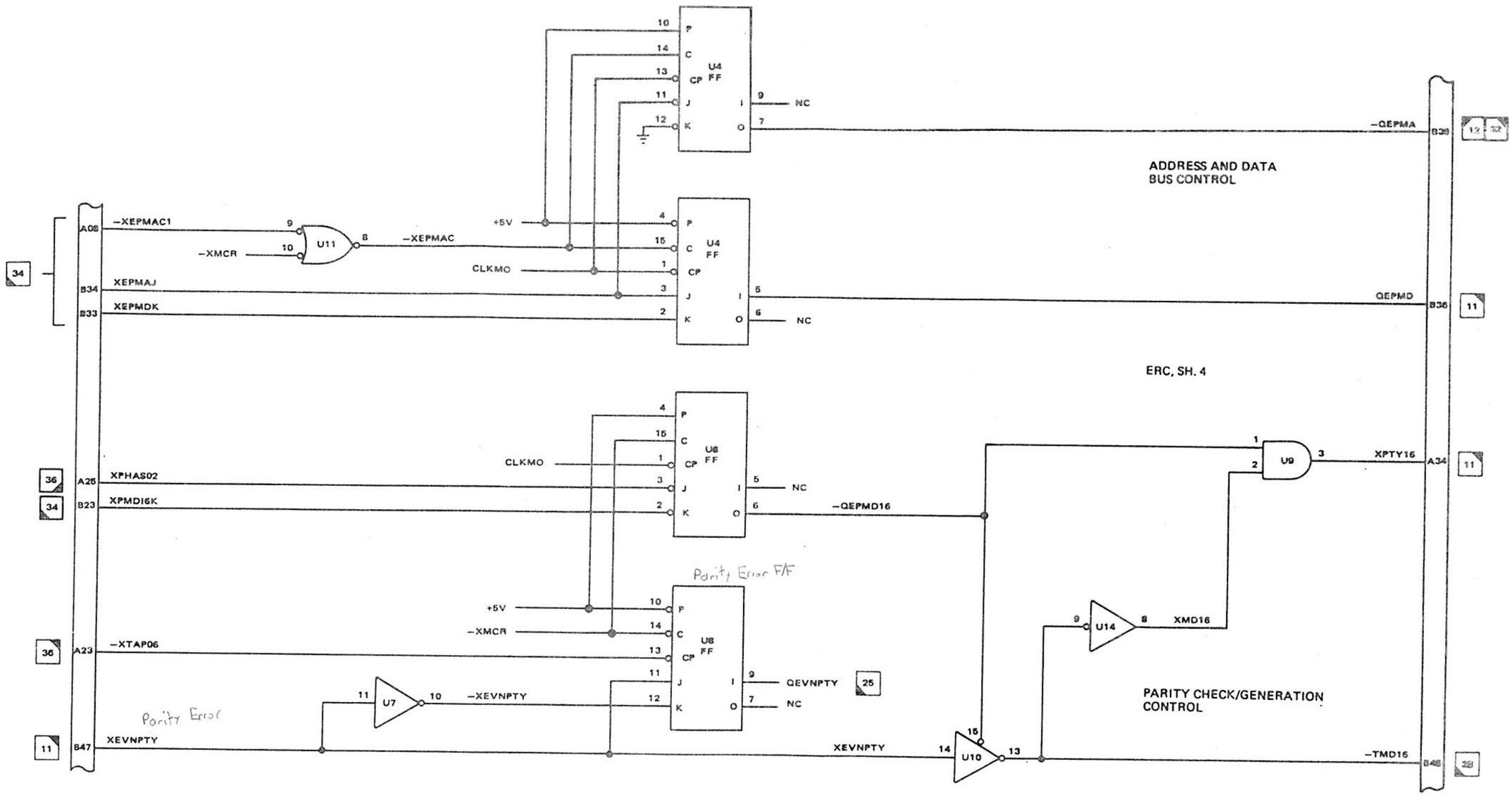
PROGRAM CONTROLLED CLOCKS (I/O CONTROL INTERFACE AND ETC)



*RD00-15 IS I/O MUX DATA FROM XCVR 29



MEMORY INTERFACE TIMING


34
A08
-XEPMAC1
9
10
U11
8
-XEPMAC
-XMCR
+5V
CLKMO
B34
XEPMAJ
B33
XEPMDK
10
14
13
11
12
U4 FF
P
C
CP
J
K
I
O
9
NC
7
-QEPMA
B38
12
32
ADDRESS AND DATA BUS CONTROL
4
15
1
3
2
5
6
NC
QEPMD
B36
11
ERC, SH. 4
36
34
A25
XPHAS02
B23
XPMDI6K
CLKMO
U8 FF
-QEPMD16
36
A23
-XTAP06
+5V
-XMCR
Parity Error F/F
10
14
13
11
12
9
QEVNPTY
25
7
NC
11
U7
10
-XEVNPTY
Parity Error
11
B47
XEVNPTY
XEVNPTY
15
14
U10
13
1
2
U9
3
XPTY16
A34
11
9
U14
8
XMD16
PARITY CHECK/GENERATION CONTROL
-TMD16
B48
38

MEMORY BANK EXTENSION CONTROL IOC, SH 1

QRD32
QRD33
U37
-QRD32-A
-QRD33-A
U18
-XIOS
U33
-XMAREE
XMARES
XSEL BK
U41 MUX
EA
EB
S2
S1
A0
A1
A2
A3
B0
B1
B2
B3
YA
YB
XMARAD
XMARBD
RDMA
QMARB
RDMB
QPSW10
QPSW08
QPSW11
QPSW09
B02
A02
B04
A03
+5V AUX
-XMCR
U47 FF
-QEPMA
A21
-QMARA
-XLDEXAD
U16 BFR
XBA06
XBA07
-TMAA
-TMAB
TP10
QMARA
-QMARB
-TDMA
-TDMB
RDMB
RDMA
U11 XCVR
XEMARO
TP11
TP16
QODE
A25
XLDMAR
U50
-CLKMAR
CLK0
XLDEXAD
A31
-XESRC3
B31
-XEBMAPS
U37
XEBMAPS
U46
-XIN
-XLDEXAD
XBA06
load external as dest
Normally low
B35
B36
XLDEX
-XRDSTP
CLK0
IOC, SH. 6
U44 FF
CLKEXT
XBA14
XBA15
QWAIT
NC
U29
-LWAIT
A49
WAIT INDICATOR
IOC, SH 6

IF: XLDMAR = 1

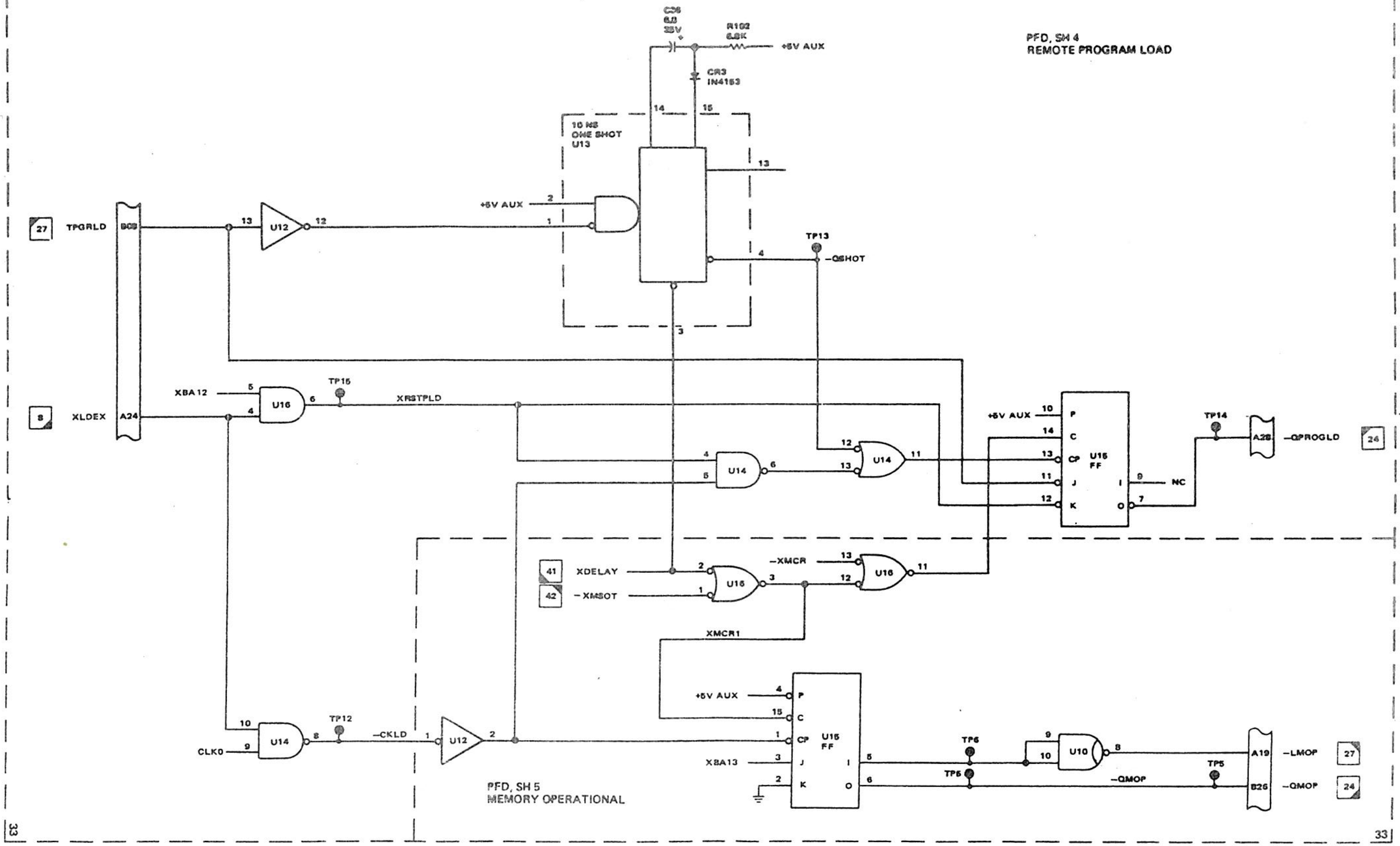
QRD32-33	XIN	*LOAD WITH:
0 0	0	TDMA/B
0 0	1	QMARA/B
0 1	X	ZERO
1 0	X	QPSW10/11
1 1	X	QPSW08/09

IF: XLDEX = 1
XBA06 = 1
QRD32,33 = 0,0

LOAD WITH: XBA06/07

OTHERWISE:
QMARA/B WILL
NOT CHANGE

MEMORY BANK EXTENSION
CONTROL LOGIC
(P/O EXT DESTINATION)



P/O EXT DESTINATION

MIF, SH 3

MEMORY WRITE CONTROL

*TO/FROM MPC IF APPLICABLE

PROCESSOR REQUEST DECODER

MEMORY ENABLE F/F

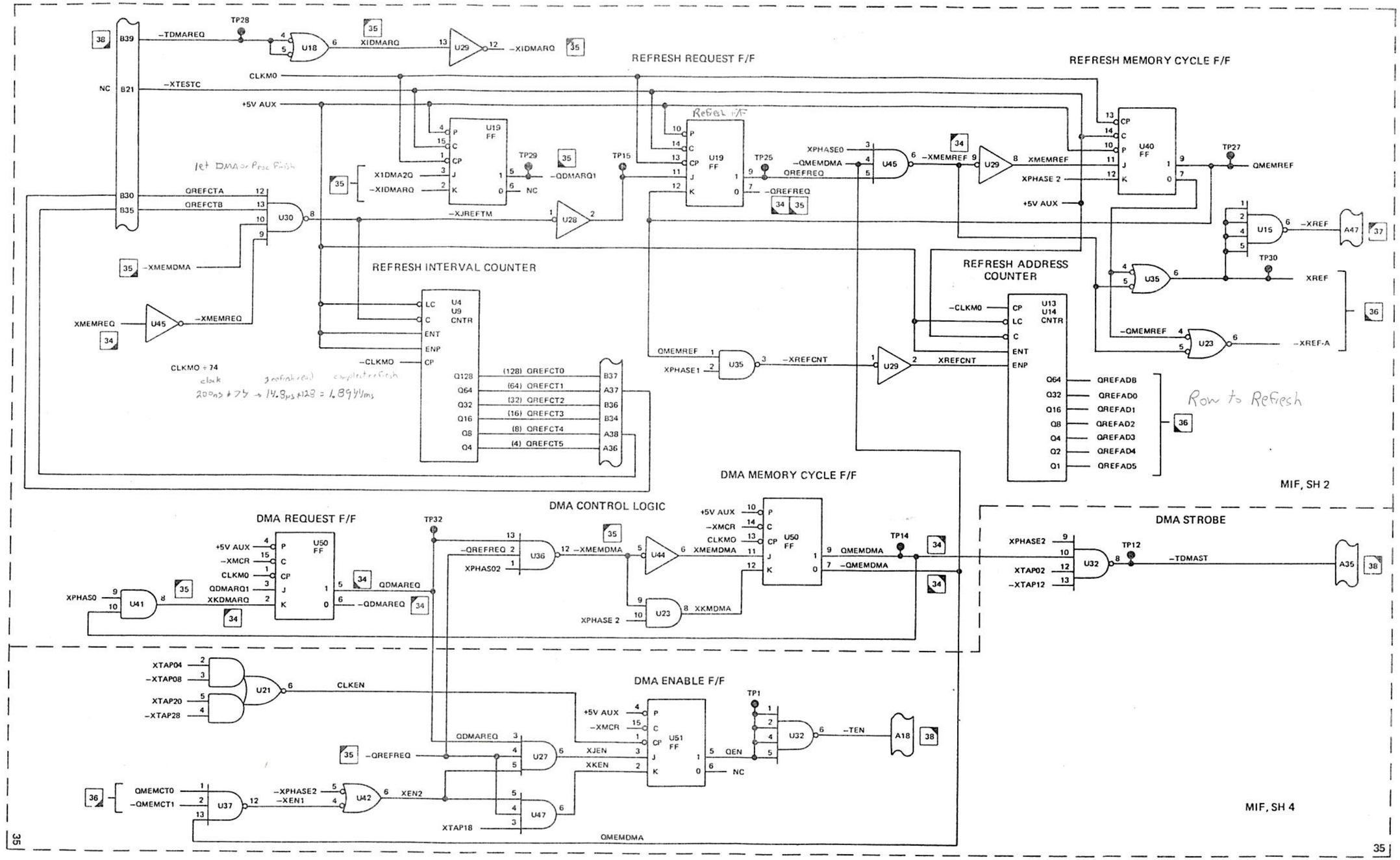
PROCESSOR MEMORY ACCESS GRANTED F/F

PROCESSOR/MEMORY INTERFACE CONTROL

MIF, SH 3

MIF, SH 1

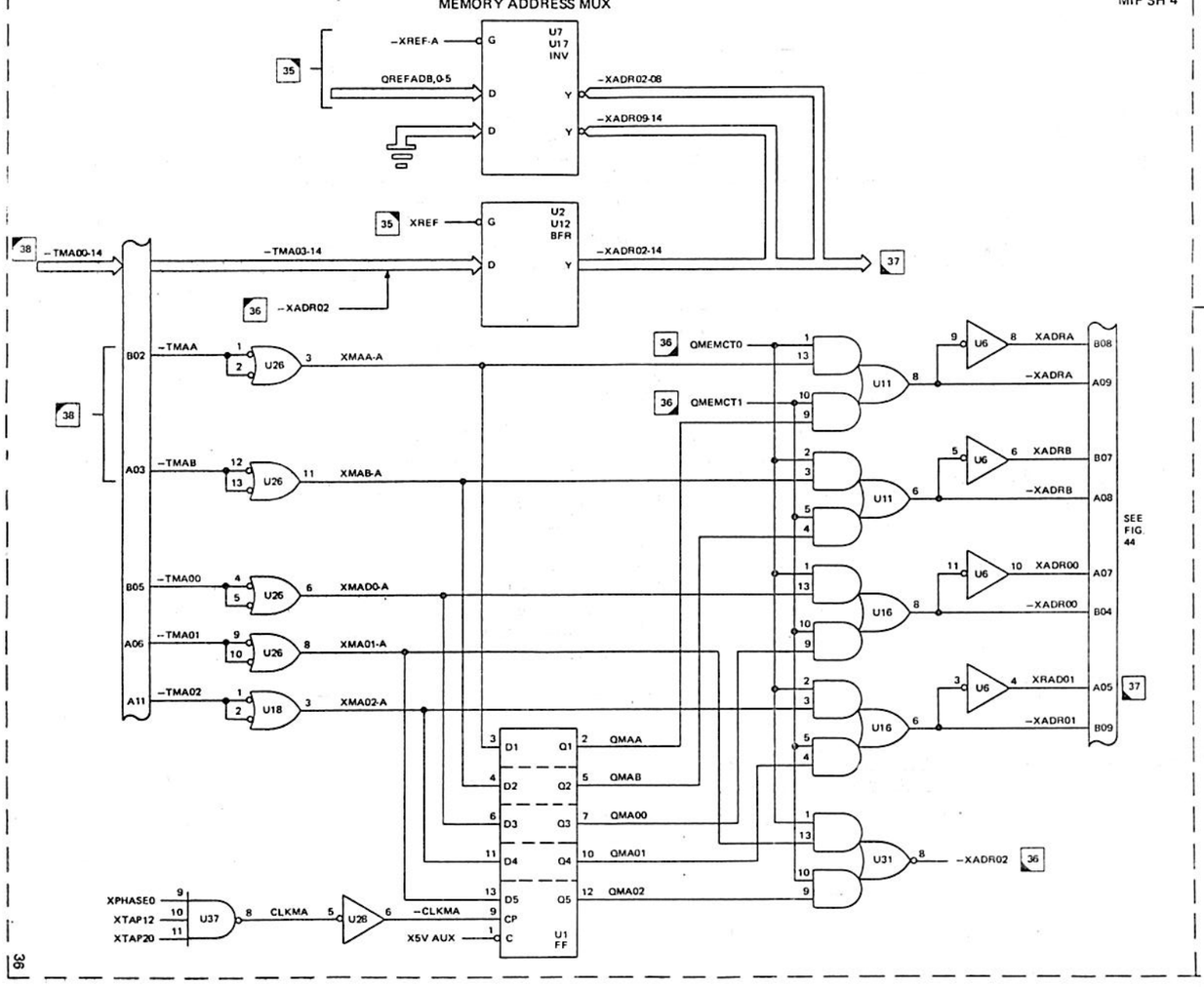
MEMORY CONTROL LOGIC

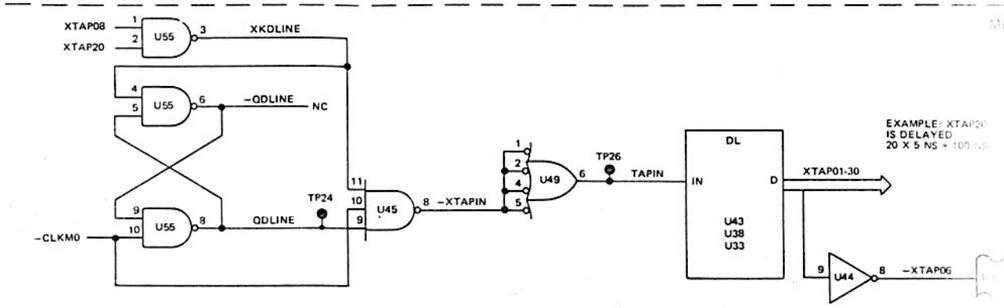


REFRESH AND DMA CONTROL LOGIC

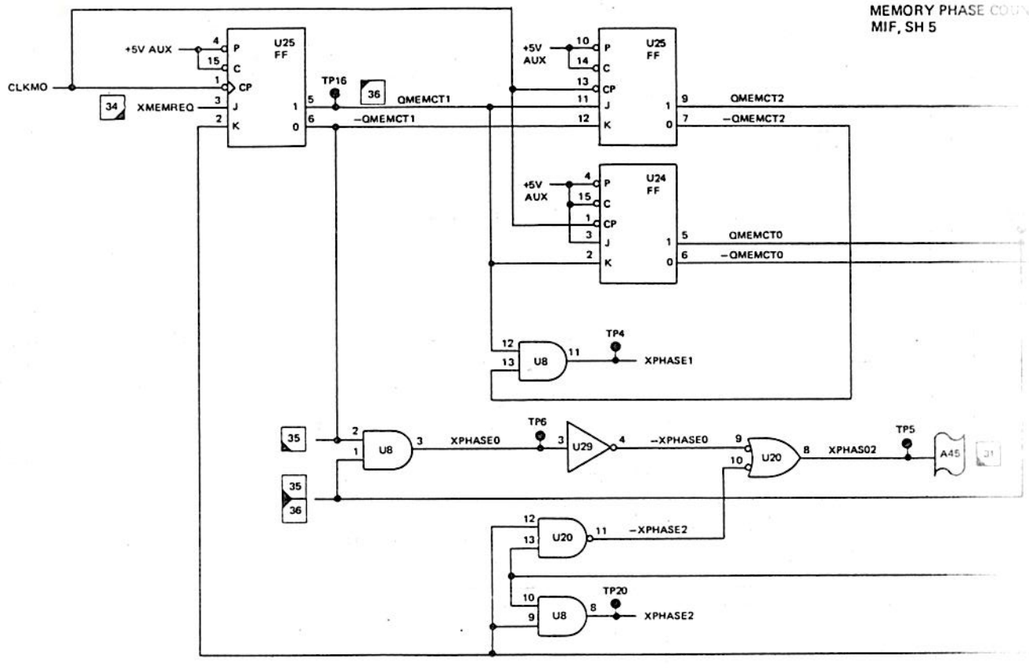
MEMORY ADDRESS MUX

MIF SH 4





MEMORY PHASE COUNTER
MIF, SH 5

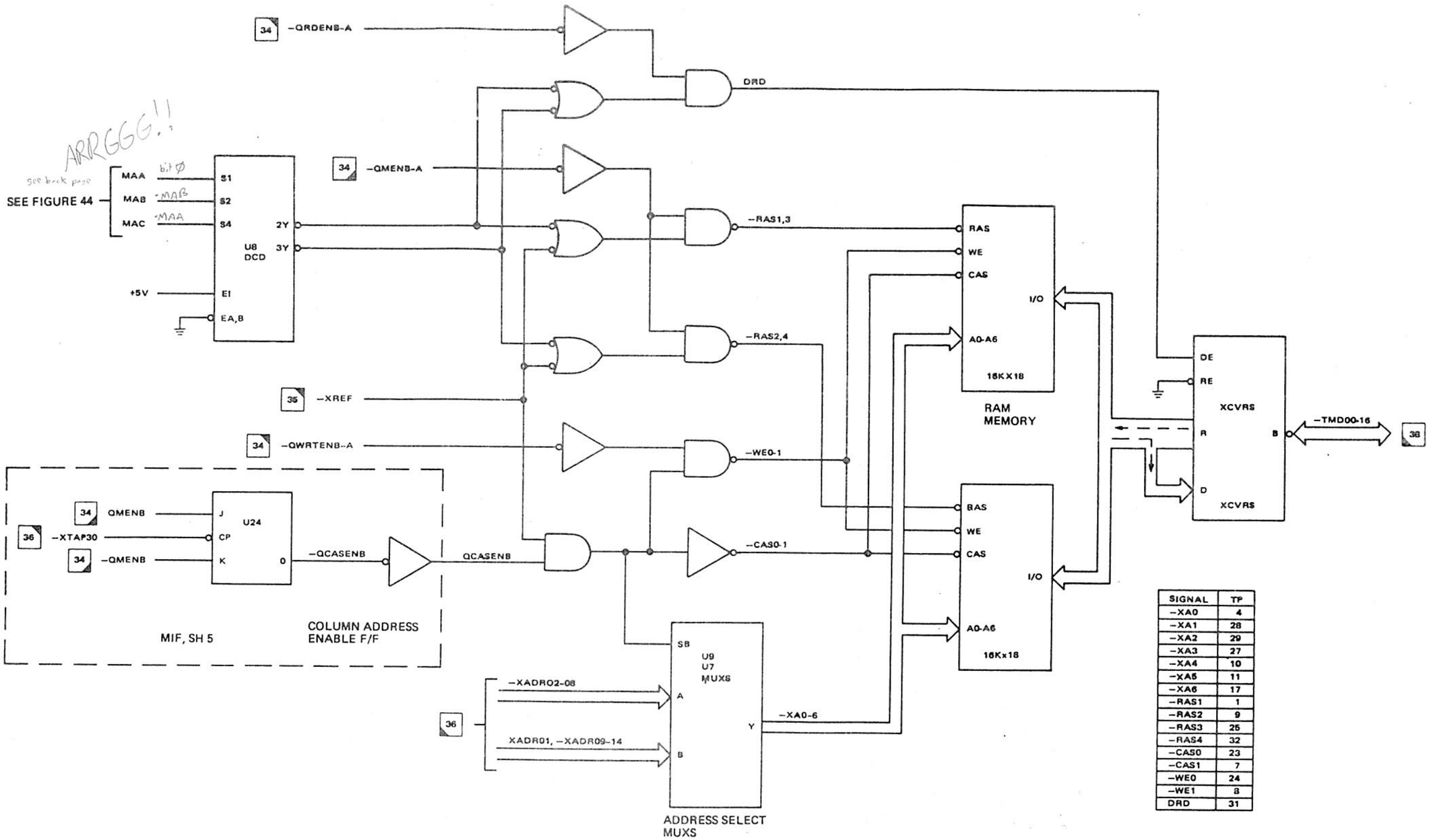


MEMORY ADDRESS AND TIMING

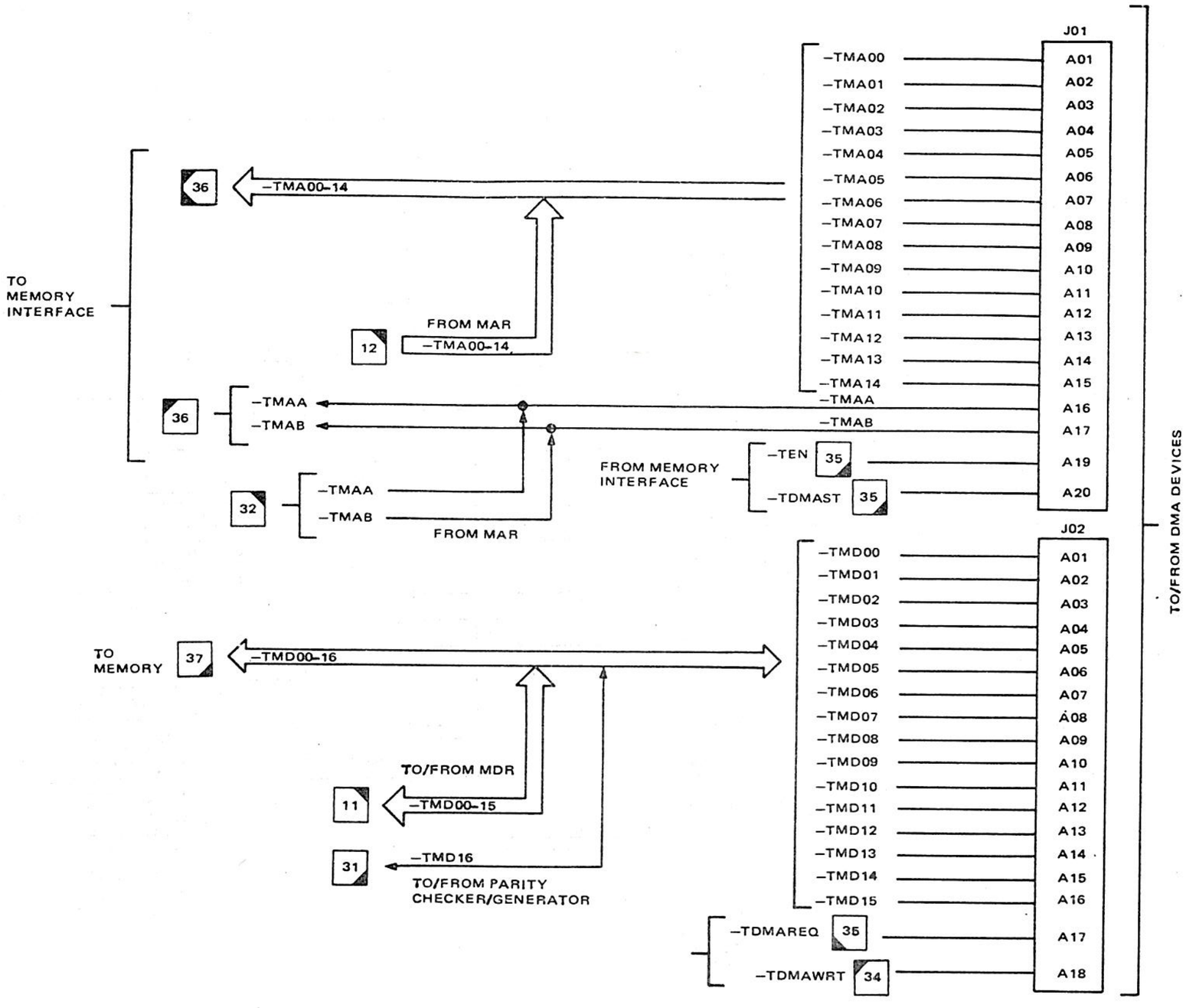
Ma C = ∅
Ma B = 1
Ma A = block

10 ← lower
11 ← upper

Mac = ∅
Mab = 1
Maa = block



SIGNAL	TP
-XA0	4
-XA1	28
-XA2	29
-XA3	27
-XA4	10
-XA5	11
-XA6	17
-RAS1	1
-RAS2	9
-RAS3	25
-RAS4	32
-CAS0	23
-CAS1	7
-WE0	24
-WE1	8
DRD	31



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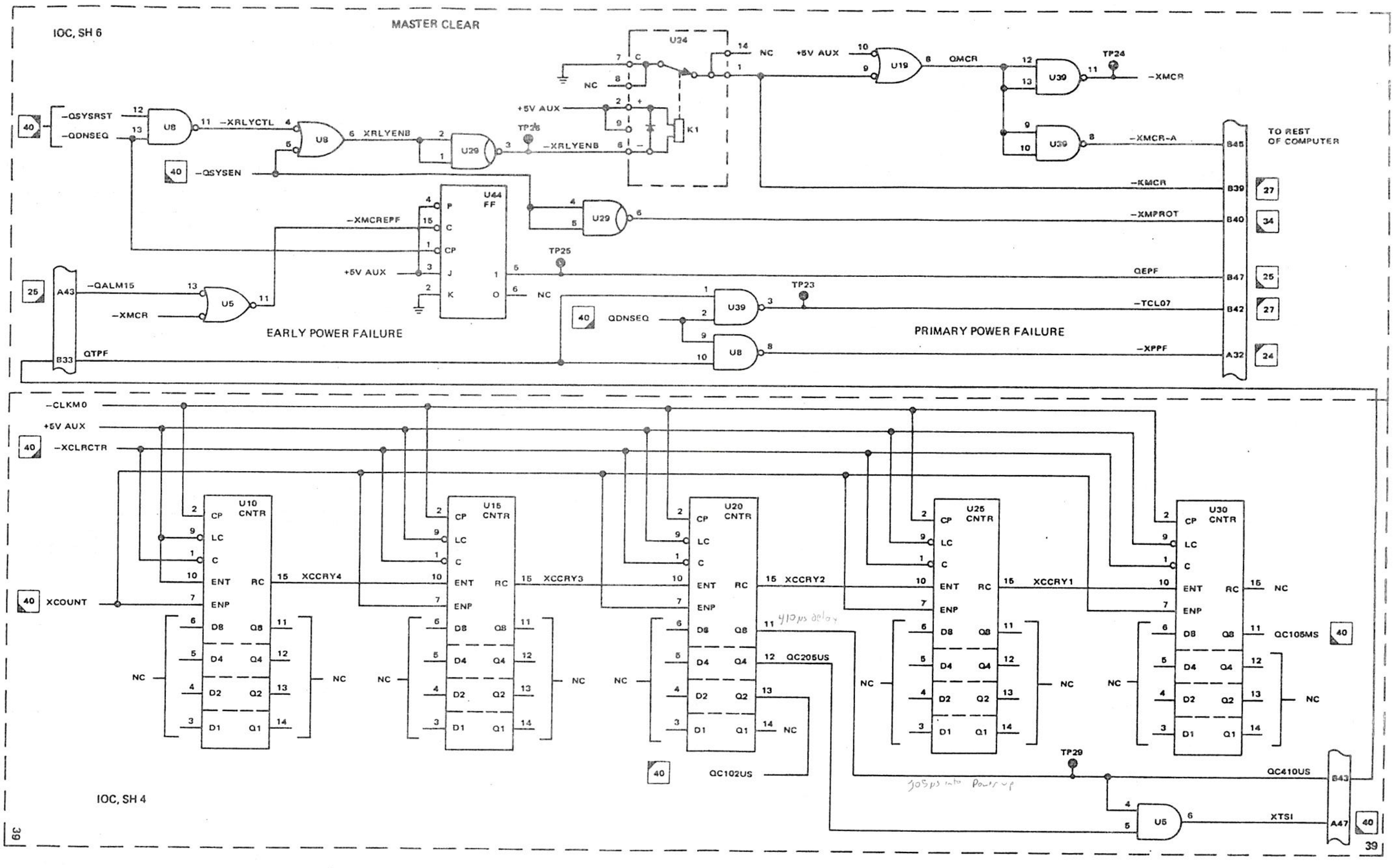
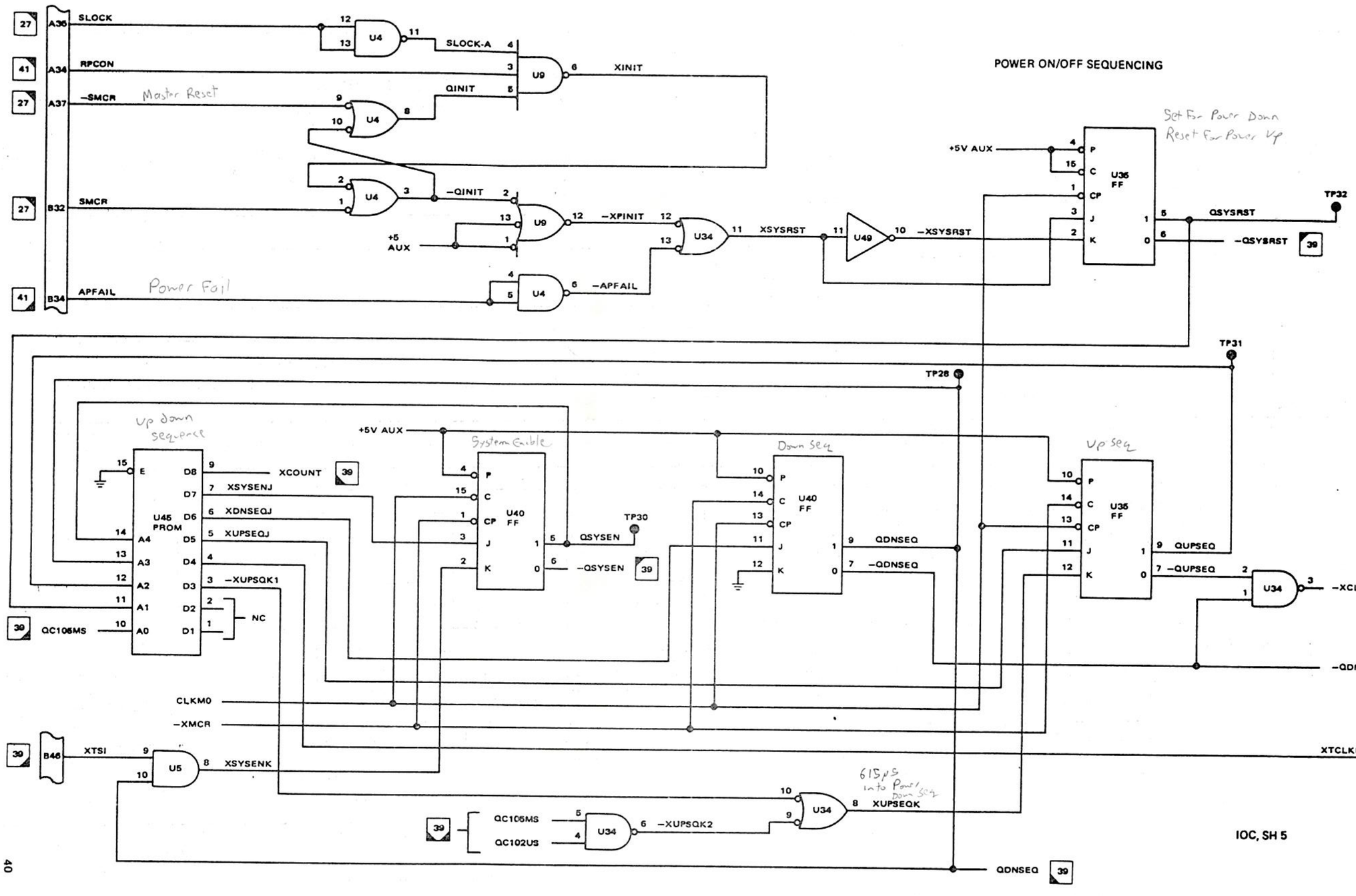
MEMORY ADDRESS AND DATA

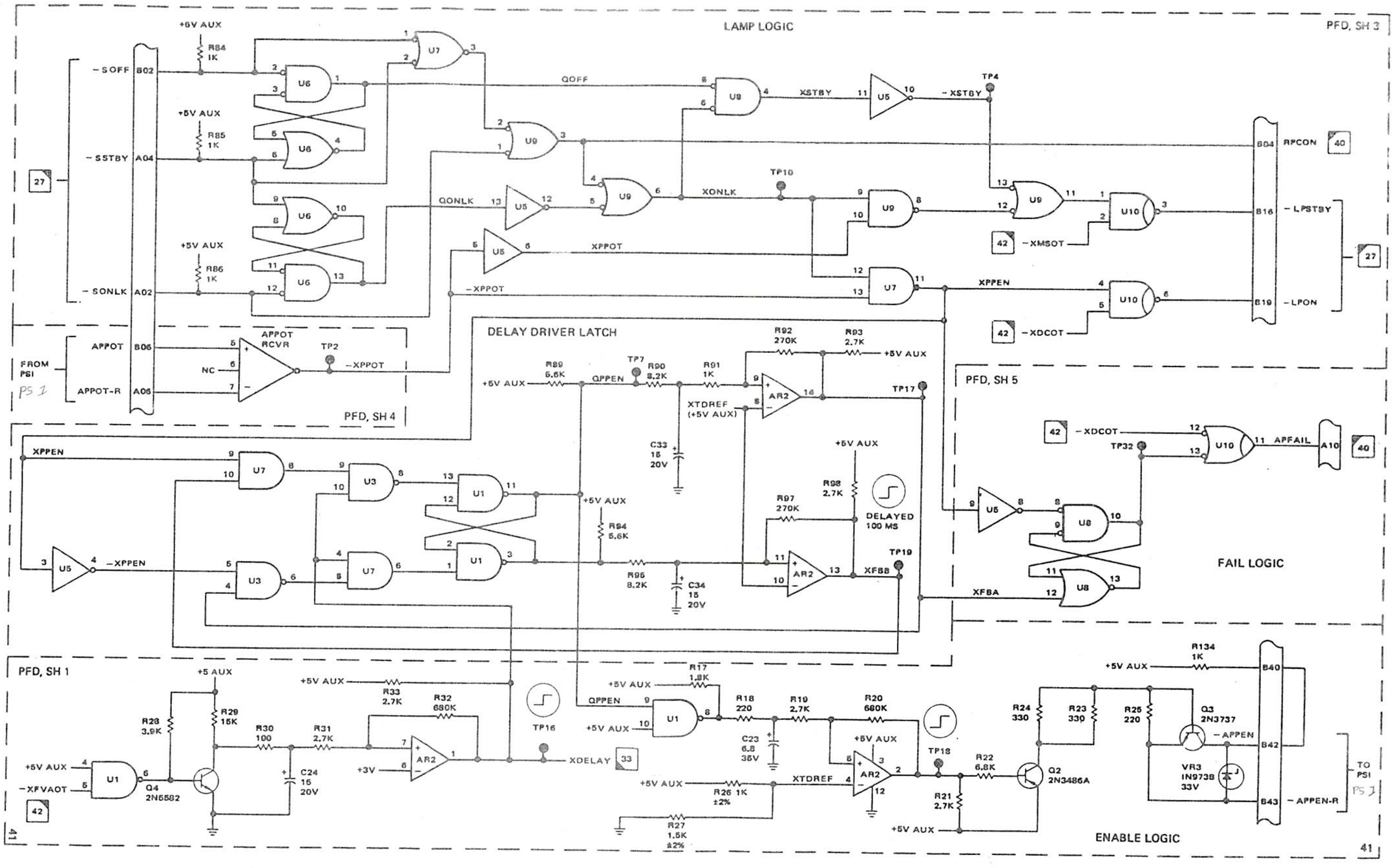


POWER UP/DOWN SEQUENCE CONTROL LOGIC (MASTER CLEAR AND COUNTER)

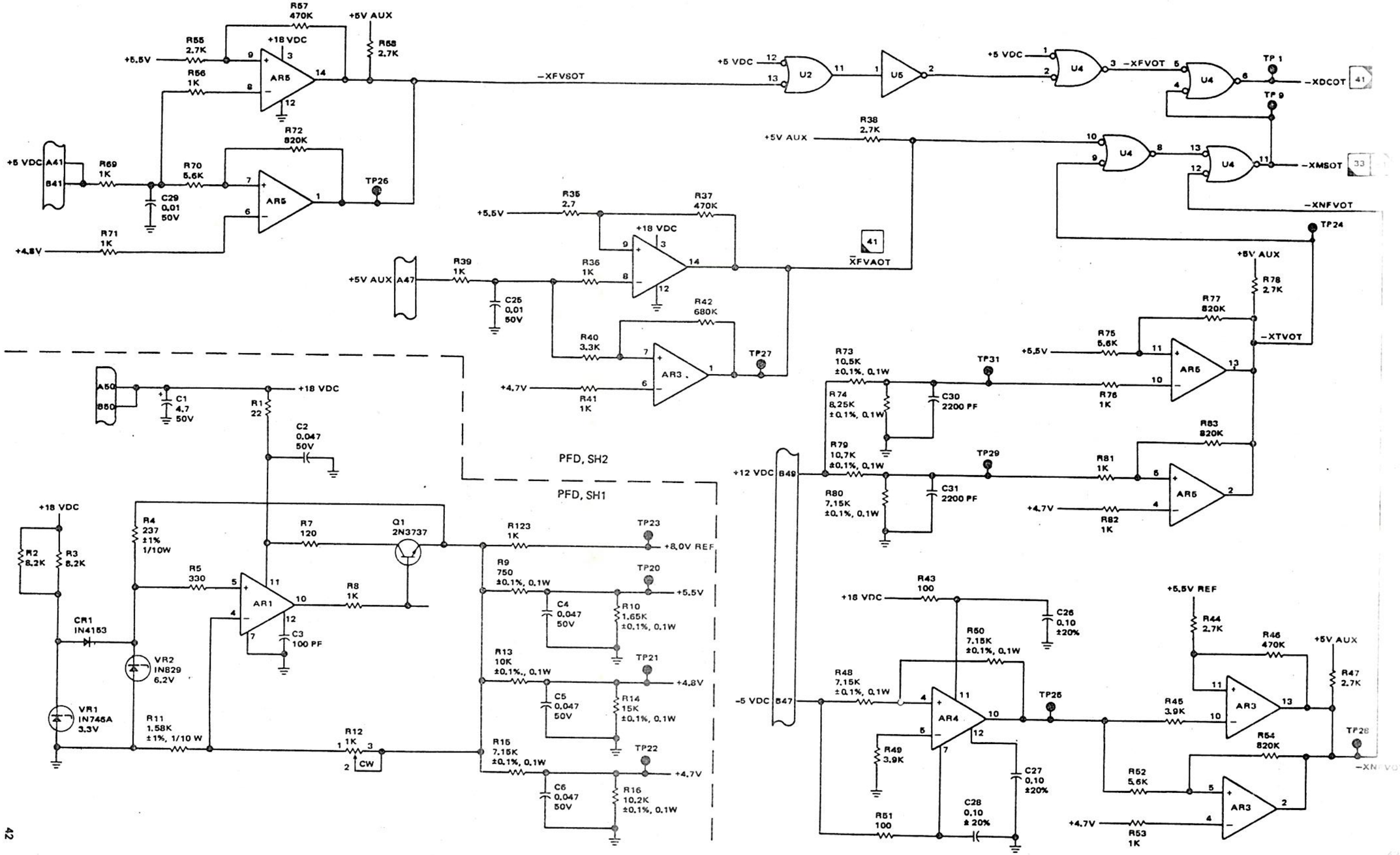
POWER ON/OFF SEQUENCING

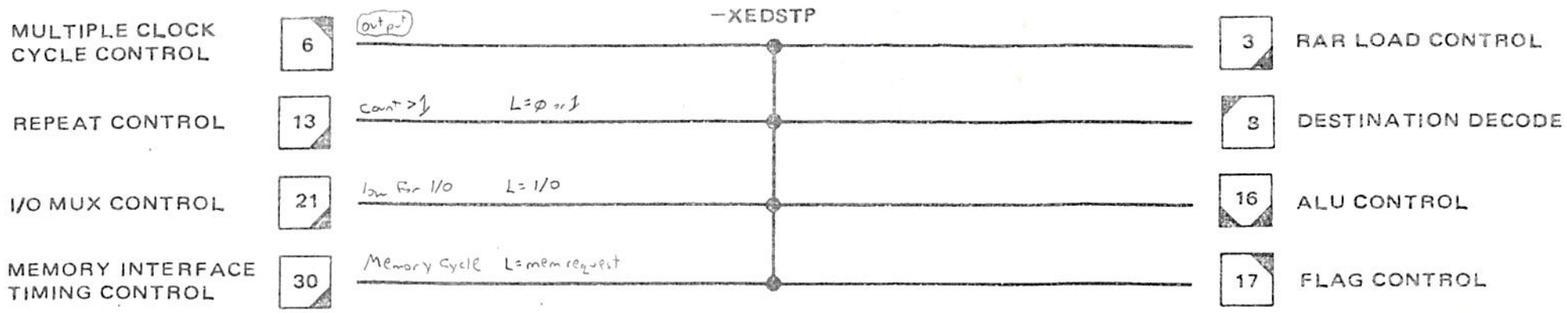


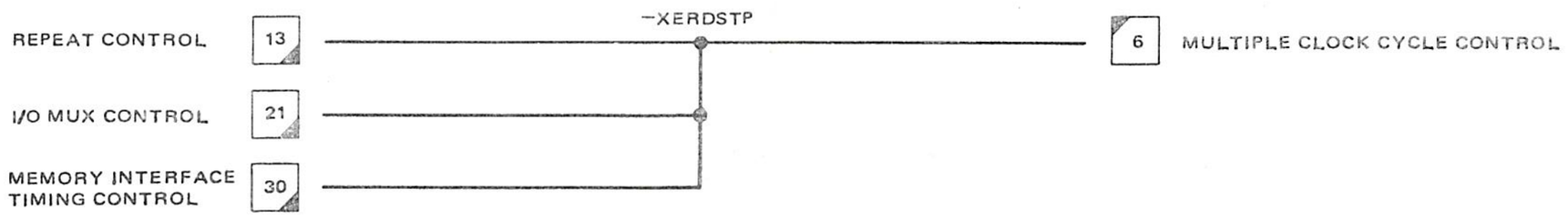
POWER UP/DOWN SEQUENCE CONTROL LOGIC (SEQUENCING CONTROL)



POWER FAULT DETECT LOGIC


R57 470K
+5V AUX
R55 2.7K
+18 VDC
R58 2.7K
+5.5V
R56 1K
AR5
-XFVSOT
+5 VDC
U2
U5
U4
-XFVOT
TP 1
-XDCOT
41
TP 9
R38 2.7K
+5V AUX
-XMSOT
33
-XNFVOT
TP24
R72 820K
+5 VDC A41
B41
R69 1K
R70 5.6K
TP26
C29 0.01 50V
R71 1K
+4.5V
R35 2.7
R37 470K
+18 VDC
+5.5V
41
XFVAOT
+5V AUX A47
R39 1K
R36 1K
C25 0.01 50V
R42 680K
R40 3.3K
AR3
TP27
+4.7V
R41 1K
+5V AUX
R78 2.7K
R77 820K
-XTVOT
R75 5.6K
+5.5V
R73 10.5K ±0.1%, 0.1W
TP31
R74 8.25K ±0.1%, 0.1W
C30 2200 PF
R76 1K
R83 820K
R79 10.7K ±0.1%, 0.1W
TP29
R81 1K
+12 VDC B49
R80 7.15K ±0.1%, 0.1W
C31 2200 PF
+4.7V
R82 1K
A50
B50
C1 4.7 50V
+18 VDC
R1 22
C2 0.047 50V
PFD, SH2
PFD, SH1
+18 VDC
R4 237 ±1% 1/10W
R7 120
Q1 2N3737
R123 1K
TP23
+8.0V REF
R2 8.2K
R3 8.2K
R5 330
AR1
R8 1K
R9 750 ±0.1%, 0.1W
TP20
+5.5V
C4 0.047 50V
R10 1.65K ±0.1%, 0.1W
CR1 IN4153
R13 10K ±0.1%, 0.1W
TP21
+4.8V
VR2 IN829 6.2V
C5 0.047 50V
R14 15K ±0.1%, 0.1W
VR1 IN746A 3.3V
R11 1.58K ±1%, 1/10 W
R12 1K
CW
R15 7.15K ±0.1%, 0.1W
TP22
+4.7V
C6 0.047 50V
R16 10.2K ±0.1%, 0.1W
R43 100
+18 VDC
C26 0.10 ±20%
R50 7.15K ±0.1%, 0.1W
+5.5V REF
R44 2.7K
R46 470K
+5V AUX
R48 7.15K ±0.1%, 0.1W
-5 VDC B47
AR4
TP25
R45 3.9K
AR3
R47 2.7K
R49 3.9K
C27 0.10 ±20%
TP28
R54 820K
R52 5.6K
-XNFVOT
C28 0.10 ±20%
R51 100
+4.7V
R53 1K

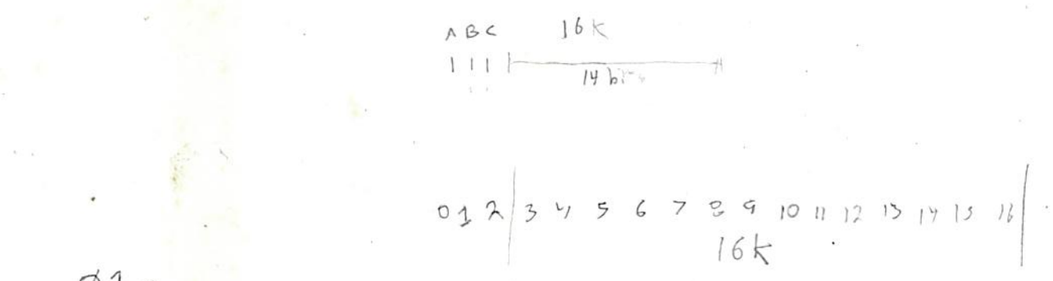




−XEDSTP AND −XERDSTP

INPUT TO DECODER ON MEMORY CARD	SLOT NO. / MEMORY ADDRESS	BANK 0	BANK 1	BANK 2	BANK 3
		18	19	20	21
S_1 MAA	XADROO	X	X	X	X
S_2 MAB	XADRB		X		X
	–XADRB	X		X	
S_4 MAC	XADRA	X	X		
	–XADRA			X	X

AN "X" INDICATES WHICH MEMORY ADDRESS SIGNAL IS CONNECTED TO THE DECODER INPUT ON THE MEMORY CARD (SEE FIGURES 36 & 37)



MEMORY CARD ADDRESS WIRING